Design of buck converter circuits operating in weak-inversion region

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***Abstract*—A 900-nA quiescent current Buck converter is implemented in standard 0.25 μm CMOS technology. The controller's analog subblocks are designed to operate in weak-inversion region to reduce quiescent current. It also implements internal compensation circuit to minimize external passive components. In order to reduce the size of an on-chip capacitor, the Miller effect is utilized. The measurement results show the successful operation of the DC-DC converter in extremely low quiescent current.**

I. Introduction

Controller ICs for DC-DC converters should be designed for low quiescent current, and for high speed operation. However, the low-power and high-speed are contradicting requirements, which make the circuit design a challenging task [1]- [6]. The general control methods can be divided into two categories. The first is the pulse width modulation (PWM) with fixed switching frequency, which makes the filtering of switching noise easier. Because of the predictable noise component, the fixed-frequency PWM control is common in noise-sensitive power management systems. The second is the variable frequency switching system, which is generally called a hysteresis controller [10]. The hysteresis controller can be implemented by comparators only, so its implementation is simpler than that of the PWM controller. Hysteresis controller's simplicity enables the implementation of low quiescent current system. However, the variable switching activity makes it very difficult to filter the switching noise.

The current industrial trend is to increase switching frequency of PWM controllers. Higher switching frequency implies that the inevitable switching noise will have less impact on low-frequency baseband area. Another advantage is the minimization of filtering inductor and capacitor sizes. Because of these advantages, the recent commercial products have switching frequency around 1MHz. In order to achieve this high speed operation, each analog component in PWM controllers requires large amount of current.

In this paper, we present a PWM controller with sub-μA quiescent current. Fig. 1 shows main blocks of the controller. Each analog building block operates in weak-inversion region to minimize current. The input bias current into each analog blocks is only 20nA and the PWM controller's minimum operating voltage is down to 0.9V. Circuit designs in weak-inversion region have been demonstrated in wide range of analog systems [7]- [9], but not in DC-DC controller design. This paper shows the results of the DC-DC controller in weak-inversion operation. Another feature of the presented controller is that its frequency compensation circuit is implemented on-chip, removing large external passive components. In order to reduce the size of an on-chip capacitor, the Miller effect is utilized [13].

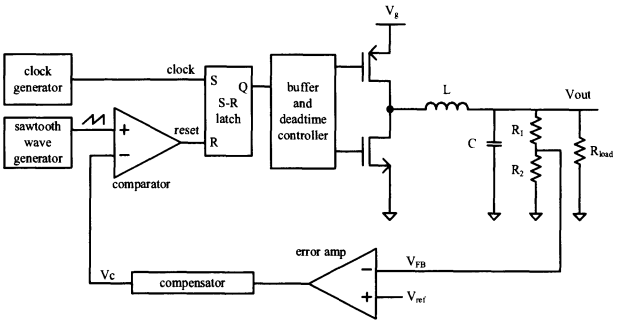

Fig. 1. Block diagram of a fixed-frequency PWM buck converter

II. Controller Design

The design of a controller should start from the stability analysis of the system. The DC-DC converter system, excluding the error amplifier and compensator, can be linearized and modeled as [11]

$$G_{vd}(s) = G_{d0}\frac{1}{(1+\frac{s}{Q\omega_0}+(\frac{s}{\omega_0})^2)} \quad (1)$$

where G_{d0} is the output voltage divided by duty ratio.

As we can see from frequency characteristic in Fig. 2 of the linearized model, The DC gain of the system is too low for accurate feedback control. Therefore, the common practice is to include high gain error amplifier as shown in Fig. 1. Since the low frequency pole of the error amplifier will have significant impact on the frequency characteristic of the system, the compensator is also required in the controller. Fig. 3 shows the frequency response of the ideal error amplifier and its respective compensator. The combined frequency response of complete DC-DC converter in Fig. 4 shows the adequate phase margin of 58^o.

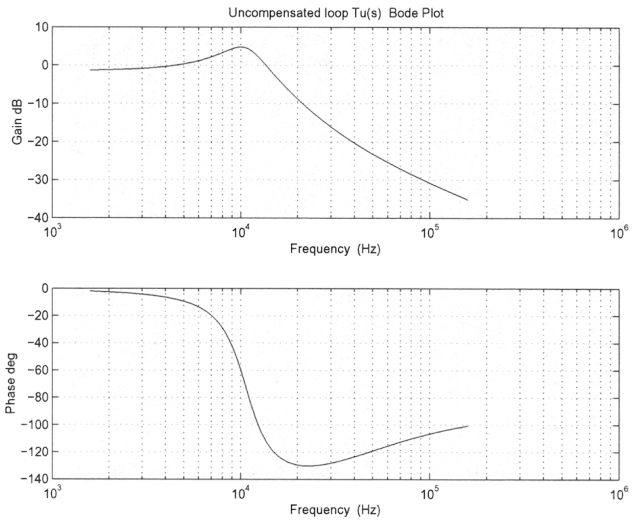

Fig. 2. Frequency characteristics of uncompensated Buck converter

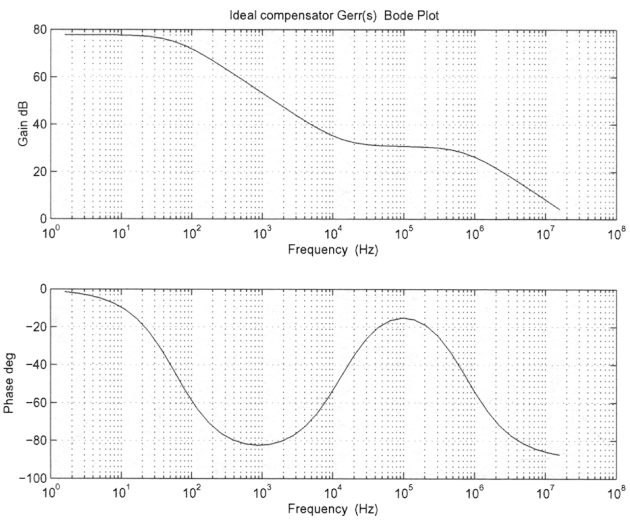

Fig. 4. Frequency characteristics of compensated Buck converter

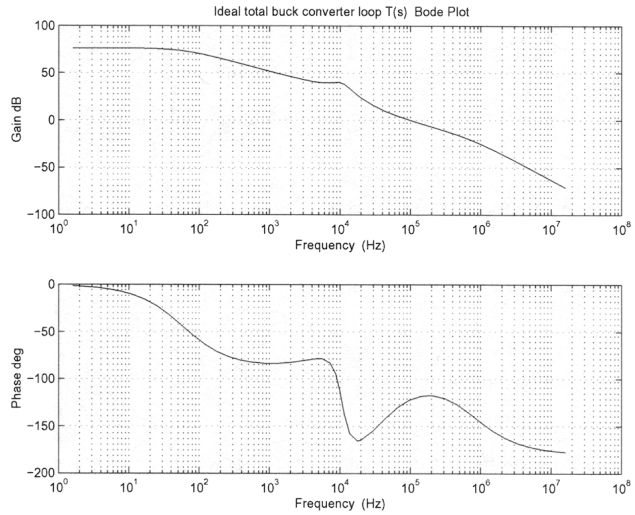

Fig. 3. Frequency characteristics of an ideal error amplifier with a compensator

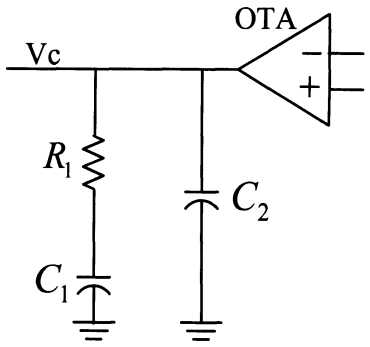

Fig. 5. Conventional OTA-type compensator

There are several conventional techniques in designing the error amplifier and compensator. Among them, one of the most popular techniques is to use an OTA with off-chip resistor and capacitors as shown in Fig. 5 [12]. In our circuit design, the Miller-compensation technique is used instead of the conventional techniques for on-chip implementation. The location of compensation pole and zero are controlled by the size of the Miller capacitor and resistor as in Fig. 6. The capacitor and resistor are designed as 9pF and 3MΩ, respectively. Table I shows the component sizes of the error amplifier. The frequency response in Fig. 7 shows that the designed error amplifier and compensator's characteristic is close to the ideal one in Fig. 3.

Fig. 8 shows the sawtooth waveform and clock generator. The current source I_b charges the capacitor C with the output voltage slope of I_b/C. The waveform will be:

$$V_{sawtooth}(t) = \frac{I_b}{C} \times t \tag{2}$$

until the clock resets the capacitor to generate the sawtooth waveform with the clock period of T_s. The bias current I_b

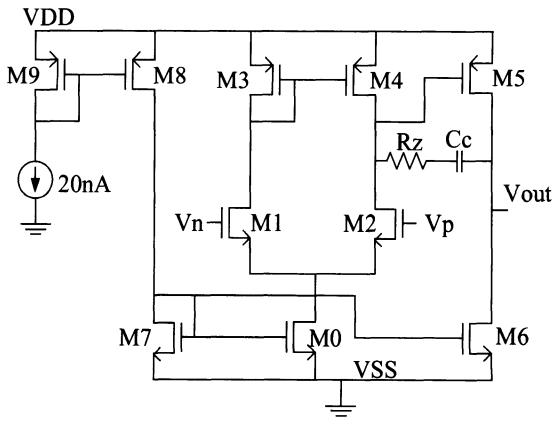

Fig. 6. Error amplifier with Miller compensator

TABLE I
COMPONENT SIZES OF THE ERROR AMPLIFIER IN FIG. 6

transistor	size	transistor	size
M0	1.0/1.7, M=4	M1, M2	1.9/1.0, M=4
M3,M4,M8,M9	2.0/1.0, M=4	M5	2.0/1.0, M=60
M6	1.0/1.7, M=30	M7	1.0/1.7, M=2
Rz	3MΩ	Cc	9pF

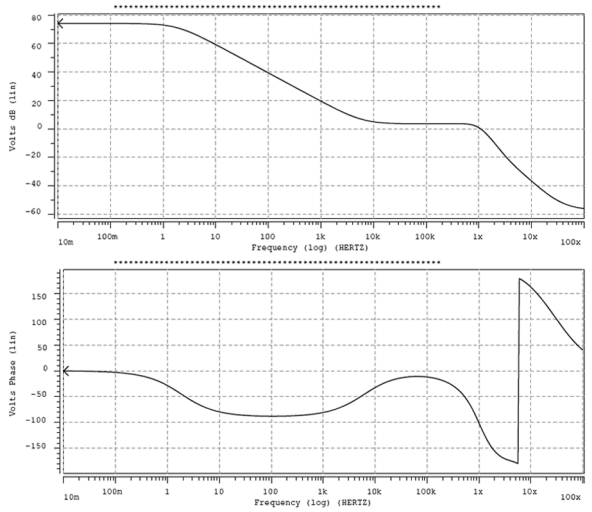

Fig. 7. Frequency characteristics of the implemented Miller-compensated error amplifier

and the capacitor C are set to 100nA and 0.1pF, respectively. An extra capacitor is also included for tuning purpose. The reference voltage V_b is controlled externally to experimentally change the clock frequency, therefore the switching frequency, of the chip.

The design criteria for comparators in PWM controllers should be different from those of the general comparators. The general design criteria would be the low offset voltage, high resolution, low delay, and no meta-stable state [13]. The input signal to general comparators would be any waveform. Therefore, the general comparators have to deal with all different situations. However, the comparators in PWM controllers have a well-defined input waveform. The sawtooth waveform will be compared with the control voltage V_c to determine the duty ratio D of the PWM output, where V_c is the output voltage of the compensator. The general comparators require significant power for high-speed operation [13]. However, if the comparator is optimzed for PWM waveforms, the power consumption of the controller can be minimized for maximum power conversion efficiency. The conventional general-purpose comparators have been used for PWM controllers [1], [2]. The characteristics of the conventional comparators are well analyzed in circuit design textbooks [13]. However, as mentioned earlier, the general design guidelines are not suitable for comparators in PWM controllers. An important observation in the operation of the PWM circuit is that the falling time of the comparator output is predictable. From Fig. 1, the falling time of the comparator is determined by the falling edge of the sawtooth waveform.

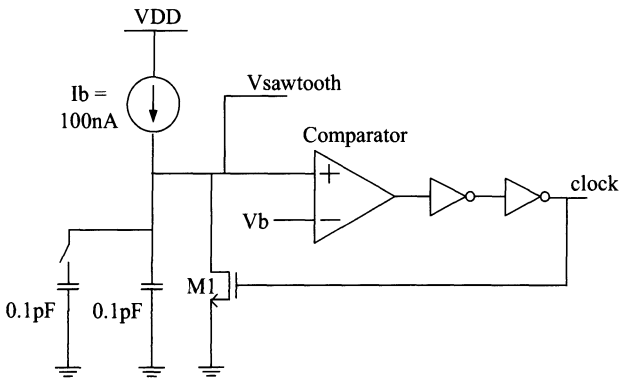

Fig. 8. Sawtooth waveform and clock generator

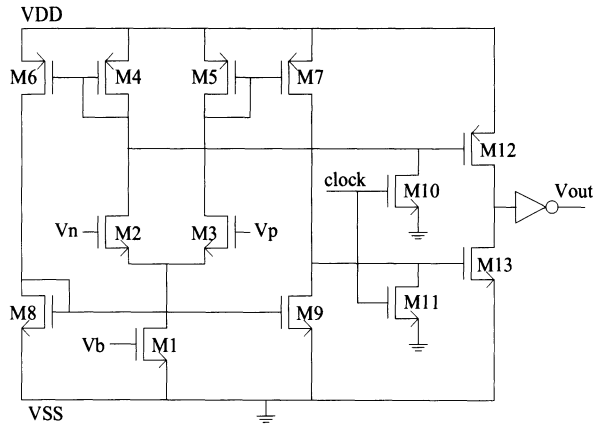

Fig. 9. Two-stage synchronized comparator

We can observe that the timing of the falling edge of sawtooth is periodic and very well defined by the clock cycle. Therefore, the accurate detection of the falling edge of the sawtooth can be simplified when we design a comparator. Instead of trying to detect the falling edge, the comparator can be synchronized by the clock. This is an important observation that would simplify the circuit design since the design effort can now be focused to minimize the rising time delay of the comparator.

The comparators in conventional PWM controllers [1], [2] do not utilize this important characteristic, so they follow the general comparator design guidelines. The first stage of the presented comparator in Fig. 9 is the conventional push-pull output OTA [13]. It has an input differential pair and current mirrors. The second stage could be similar to that of the conventional two-stage comparator by using the common-source amplifier with a current-source load. In other words, if M12 in Fig. 9 is driven by a DC bias voltage, the overall architecture will be similar to the conventional comparator except that the first stage is a push-pull type. However, the problem of the conventional second stage is that it consumes large current

because the current-source load is always on. Therefore, in order to avoid this current loss, the load current of the second stage is adaptively controlled in the new comparator, so that M12 and M13 operate in a class-AB style. The maximum current supplied by M12 is:

$$I_{max,M12} = \frac{(W/L)_{M12}}{(W/L)_{M4}} \times I_{M1} \quad (3)$$

where I_{M1} is set to 40nA in our implementation.

TABLE II
TRANSISTOR SIZES OF THE SYNCHRONIZED COMPARATOR IN FIG. 9

transistor	size	transistor	size
M1	1.0/1.7, M=4	M2, M3	0.32/0.24, M=6
M4-M6,M12	0.32/0.24, M=2	M7	0.32/0.24, M=14
M8-M11,M13	0.32/0.24, M=2		

Since its maximum current is limited, the falling speed of the comparator might be also limited. However, as previously mentioned, the falling time is synchronized by the clock in the designed circuit, the operation speed of M12 is boosted significantly. The speed of M13 is important for high-speed and accurate operation of the comparator. Unlike M12, the pull-down transistor M13 has a wide swing at its gate, so its driving capability is high. According to the observation earlier, we can ignore the role of the comparator to detect the negative slope. Instead, built-in reset switches, M10 and M11, are implemented, which are controlled by the same clock signal that resets the sawtooth signal as shown in Fig. 8. Now the comparator does not detect the negative slope of the input waveform, but it detects only the positive slope of the sawtooth waveform. The transistor sizes are summarized in Table II.

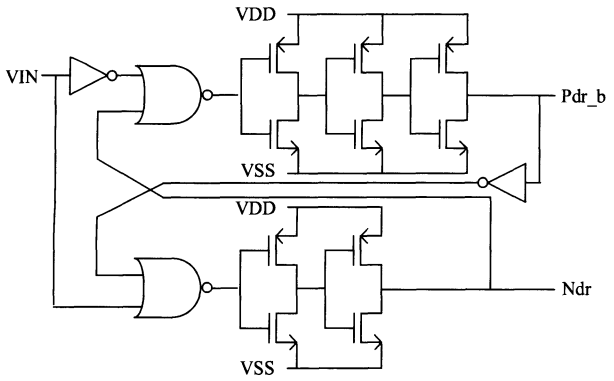

Fig. 10. Deadzone control and drive buffer circuit

Since the Buck converter has both PMOS and NMOS power transistors, deadtime control is required to prevent short-circuit power consumption. Fig. 10 shows deadtime control and buffer circuits. Pdr_b drives PMOS power transistor as an active-low signal, and Ndr drives NMOS power transistor as an active-high signal.

III. EXPERIMENTAL RESULTS

The controller is fabricated using standard 0.25 μm CMOS process. The chip size of the controller is 780 $\times$ 850 μm^2 including the power transistors as in Fig. 11.

TABLE III
OVERALL CHIP PERFORMANCE

Technology	0.25μm standard CMOS process
Die size	780 $\times$ 850 μm^2
Switching frequency	500kHz to 1.1MHz
External LC filter	L=10μH, C=22μF
Peak efficiency	91%
Input voltage range	0.9 to 2.5V
Output voltage range	0.4 to 1.8V
Output current range	$\leq$ 220mA

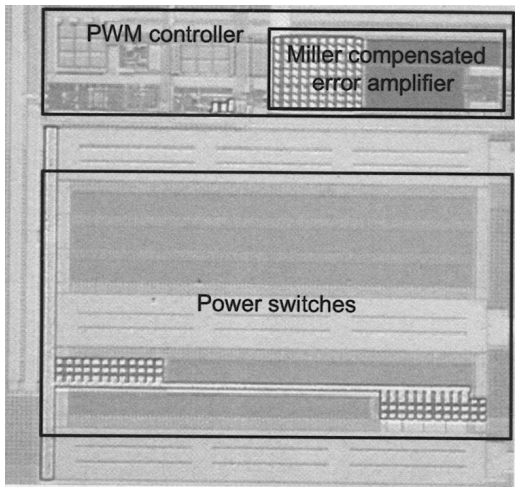

Fig. 11. Chip photograph

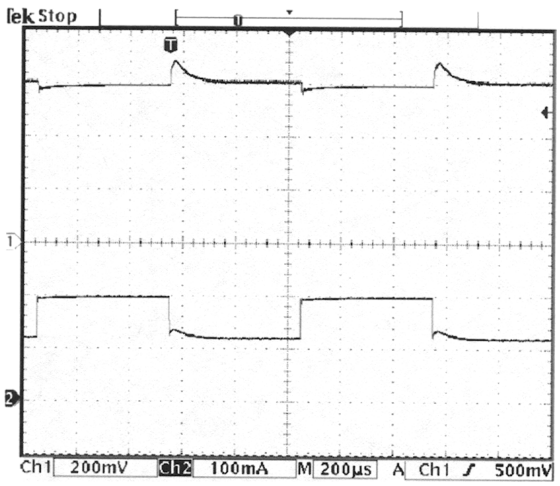

Fig. 12. Transient response for load current variation

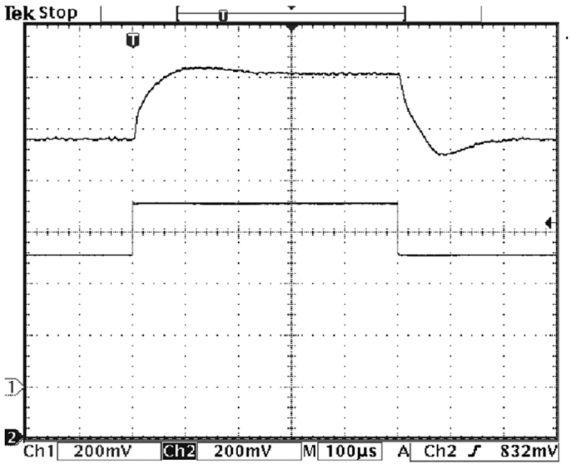

Fig. 13. Transient response for reference voltage variation

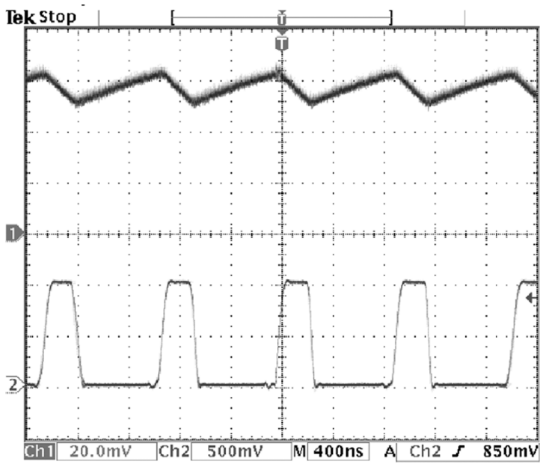

Fig. 14. Output ripple voltage and comparator output

The bias current of only 20nA is supplied from the test board into the chip. The operation voltage is measured as from 0.9V to 3V, and the switching frequency can be controlled by adjusting the bias voltage V_b of the clock generator in Fig. 8. The controller operated successfully for switching frequencies of 500kHz to 1.1MHz. The overall performance is summarized in Table III.

Fig. 12 shows the transient response for load current variation of 125mA to 200mA, while the input and output voltage are set to 2.5V and 0.6V respectively. As the waveform indicates, the output voltage reacts to step changes of the load current but quickly returns to the original value by the feedback system control, maintaining a stable voltage. Fig. 13 is for the reference voltage variation. The reference voltage is changed from 0.7V to 0.9V as the lower trace in Fig. 13. The voltage scaling resistors R_1 and R_2 in Fig. 1 are set to 150kΩ and 450kΩ, respectively. Therefore, output voltage follows the reference voltage by the ratio of the scaling resistors. The output voltage ripple is shown in Fig. 14 with the clock signal in the lower trace. It shows a stable operation of the circuit at the clock frequency of 1MHz for the input voltage of 1V and the output voltage of 740mV.

IV. Conclusions

The ultra-low quiescent current DC-DC converter is designed and demonstrated. The analog subblocks operate in weak-inversion region to minimize current. The quiescent current of the presented controller is the lowest current reported [4] to the best of authors' knowledge. Details of the analog blocks are explained for low quiescent current operation, and experimental results are shown. The successful operation of the chip proves that the DC-DC converters can operate in very low-power conditions.

Acknowledgements

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