Deep Submicron Technologies for HEP

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ABSTRACT

This review paper discusses the applicability of advanced deep submicron technologies in the High Energy Physics environment. Most of the read-out electronics required for the generation of experiments scheduled for the future LHC accelerator has to be implemented as custom or semi-custom ASICs; the choice of an appropriate technology for the design of these components has wide ranging technical and economical consequences. In addition to requiring the integration of millions of channels at low cost and extremely low power, experiments demand the availability of components with an unprecedented level of radiation hardness - even when considering the technologies developed for space and military applications - and reliability.

State-of-the-art deep submicron (< 0.35 µm) technologies can offer several technical and economic benefits. Such advantages come from the high volume, high yield, low cost per wafer fab-lines in which these technologies are produced, combined with the higher density, intrinsic radiation tolerance and low power inherent in deep-submicron CMOS. Nevertheless a number of difficult obstacles still face designers who are trying to find an optimal solution for LHC components.

1 INTRODUCTION

Few fields of technology are changing as rapidly as solid-state circuits. Computer components, their interconnections, consumer and telecommunication electronics are all gaining performance – or decreasing their price/performance ratio – at an exponential rate, thanks to a 'continuous revolution' in the field of microelectronics. LHC is coming at a time when Moore's law is still widely believed to be valid. The semiconductor industry has achieved a 25-30% per year cost reduction per function over the past three decades. While this offers enormous advantages to the quick engineer, it also requires management to understand how to take advantage of this revolution with a minimum of risk.

Until recently High Energy Physics could not take any advantage of the developments in the field of commercial VLSI, as it was widely believed that radiation would damage irreversibly circuits which were not manufactured with specially adapted processes, as to become insensitive to radiation effects. Recent investigation in the area of deep-submicron technologies are now showing [1] that, by combining appropriate layout techniques with new 'standard' technological advances, one can develop designs that are robust to radiation, thereby removing the primary obstacle to the utilization of these technologies in the radiation environment of some future experiments.

On the other hand, advanced technologies are today used in industries which are organized in a way vastly different than the HEP community, with typically tens if not hundreds of designers assigned to every aspect of a project and with a hierarchical organization in order to manage teams of many creative individuals.

Time-to-market is the factor driving most industrial projects. Very large investments in technology and design have to be amortized quickly, and new capital has to be raised to invest in the next – more complex and demanding – technology. In some markets products succeed or fail commercially due to just a tiny time difference in their introduction, which can be as short as a few months.

To profit from this Pandora's box situation, HEP must understand how to handle such technologies and what needs to be put in place to minimize the risk of not being ready for the day the LHC accelerator will be turned on.

2 TECHNOLOGY ASPECTS

The early adoption of a technology inevitably implies that many of the infancy problems of a technology are not yet solved and that a painful learning curve will have to be faced.

The technology generation which some designers are today considering for LHC experiments is basically a digital 0.25 µm CMOS technology. Today a handful of manufacturers have the technical capability of fabricating ASICs based on such a technology, while several more use it to build their 64/256 Mb DRAM and microprocessors; the largest semiconductor manufacturer worldwide has recently announced that all its products starting from 1998 will be produced on 0.25 µm lines or better and describes the basic process in [2].

RD-49 has recently been evaluating two different 0.25 µm CMOS technologies.

	1997	1999	2001	2003
Min gate L [nm]	250	180	150	130
Tox [nm]	5	3-4	3	2-3
V_{DD} [V]	2.5	1.8	1.5	1.2
f_t [GHz]	20	30	35	40

Table 1 SIA 1997 Forecast for some parameters in VLSI technology (from Ref 3).

Assuming that LHC will start as scheduled in the year 2005, and looking at the forecast issued last year by the Semiconductor Industry Association (SIA)[3], industry at that time should be able to produce ICs with minimum line-width more than a factor of 2.5 - or two generations - denser (see Table 1).

Considering that technologies such as a 0.8 μm CMOS (about 3 generations behind 0.25 μm) are today rapidly becoming obsolete, one could conclude that by the start of LHC even today's jewel will probably be obsolete.

2.1 *NEW FEATURES*

Deep submicron CMOS introduced several new features in devices; moreover, not all the features listed below are necessarily introduced by all manufacturers:

- Local Oxidation has been replaced by Shallow Trench Isolation (STI), this has changed the profile of devices and potentially their leakage current characteristics. In the measurements performed so far on an STI technology, no degradation has been observed compared to LOCOS, some recent measurement indicate even that devices with non-enclosed structure consistently maintain a leakage current at pre-irradiation levels up to 200 Krad.
- Dual gate implants are now standard, and allows the individual threshold adjustment of N and P devices.
- Thin gate oxides are standard at about 45-60 Å for 0.25 μm technologies and are fundamental to their total dose radiation hardness.
- Shallow Source/Drain and sometimes complex Lightly Doped Drain (LDD) structures are required to minimize short channel effects.
- Silicided Source and Drain are necessary to reduce the series resistance to the metal contact and offer an extra free metal level. The resistance of polysilicon is also often reduced with similar techniques. This step may sometimes be undesired for analog applications, where high resistivity polysilicon or wells might be needed for implementing resistors; and may be optional (masked off) in some processes.
- Lower Supply Voltage has the largest practical impact on designers. V_{DD} of 2.5 V is standard at 0.25 μm gate length and this requires designers to avoid configurations with more than two devices in series. On the other hand, some manufacturers offer options for NMOS devices with a threshold voltage close to 0 V, for application in analog circuits. In addition, as technology is scaling down and the ratio between supply voltage and threshold voltage (V_t) becomes smaller, concern about leakage current for multi-million transistor chips is increasing. Manufacturer are actively looking at processes with two V_t voltages, low V_t for high performance but leaky circuits, and high V_t for low power and slower circuits, or at modulating the V_t through action on the substrate potential [4]. Feasibility studies of large dynamic range analog circuits at the reduced supply voltage are under study and practical solutions are being investigated.
- The number of metal interconnect levels is growing to 5 or more, as commercial microprocessors are definitely limited by the technology's interconnection capacity and not by the number of transistors. While this development is vital for most commercial circuits, it has a relatively small impact on HEP designs, where mixed signal circuits are more common, except for such density critical applications such as pixel detectors.
- Last but not least, the interconnection to the external world is also changing, as more manufacturers are introducing advanced bonding techniques, using bump-bonding or tape techniques. Wire bonding to 70-80 μm pitch is becoming available and low-cost bump-bonding to 230 μm (area array pitch) is also available.
  This change can have a profound impact on HEP ASICs if the new packaging and interconnect techniques are mastered in time. An important fraction of the cost of front-end detectors is contributed by the wire-bonding. A large saving can potentially be achieved by using more automated, and more reliable bonding techniques. The introduction of these bonding technologies nevertheless demands that designers introduce testability features based on scan-path in their circuits.
- Some foundries offer a BiCMOS option, even with exotic SiGe bipolar devices. Such technologies - with bipolar f_t in the range of > 50 GHz - are targeted at very high speed RF and telecom components (see for example [5]).

2.2 *RADIATION-HARDNESS: WHAT IS KNOWN*

The utilization of enclosed gate MOS devices can be traced back to the early days of commercial field effect devices, when it was immediately recognized that making transistor profiles which would not leak was difficult [6]. The same layout techniques has been used with a commercial technology and has proved to be effective in eliminating radiation induced leakage.

The threshold voltage shift induced by charge trapped in the gate oxide can instead be eliminated by using very thin gate oxides (< 7 nm) which are 'natural' in deep submicron technologies [7].

Experimentally we measured threshold voltage shifts of < 5 mV up to 1 Mrad (SiO_2) and < 30 mV up to 10 Mrad for both N and P devices in a technology with a 5 nm gate oxide [8]. At the same time, leakage currents are maintained to pre-irradiation levels for all enclosed devices. Finally, a g_m degradation of < 7% was measured at 30 Mrad.

Figure 1 shows for example the robust behavior pre-and post irradiation of a ring oscillator implemented with enhanced layout rules.

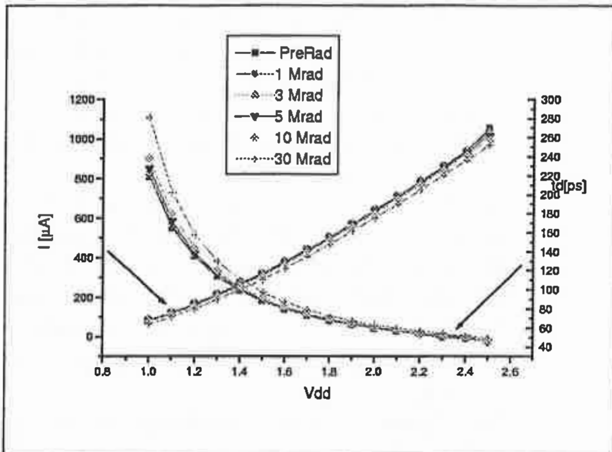

Figure 1 Delay per stage and supply current for a 1001 element ring oscillator in 0.25 µm technology as a function of supply voltage and total dose.

2.3 DIFFICULTIES AND CHALLENGES

Every new technology brings along a set of new design challenges. In the commercial field the deep-submicron generation has exposed the wiring delay problem to the digital designer and new technologies (for an example of a high performance multi-wire thickness technology see [9]) and tools instructing the synthesis tool to handle wiring delays as a principal constraint are appearing.

2.3.1 MODELING

Enclosed devices require special care in circuit modeling. Enclosed field-effect devices do not exhibit symmetry between source and drain and the modeling of an effective W/L ratio requires special care [10].

In addition, first generation deep-submicron device models are issued by industry mainly for digital application, and the device modeling might be less accurate than needed for an analog circuit.

An example of the accuracy that a designer might expect from a BSIM3 model is given in Figure 2.

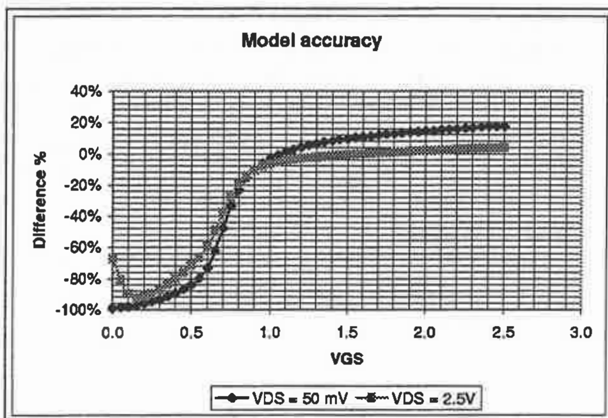

Figure 2 Comparison of measured and simulated data for a normally drawn 10/0.28 µm NMOS device in linear and saturation region. To cancel out any process dependent effect, the simulated data curve was normalized with a process sigma such as to maximize the accuracy in the region $V_{GS} > 1.0V$ and $V_{DS} = 2.5$ V.

In addition, process spread for analog parameters is still poorly defined and will require the submission of many test wafers to become better known.

The figure below illustrates also that the short channel effects are very important at short channel lengths and that hand calculations based on the simple $I_{DS} \propto (V_{GS}-V_t)^2$ law can be substantially incorrect.

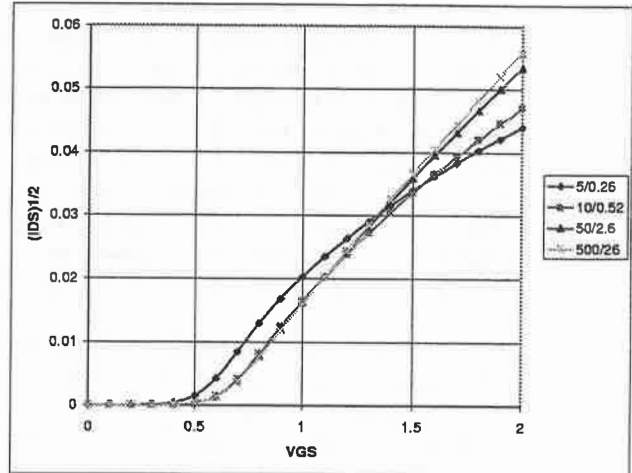

Figure 3 Departure from simple $(V_{GS} - V_t)^2$ law for short channel devices

Published data [11] report a potential large difference (25% to 56% between wafer center and edge) in performance of chips on the same wafer and the exact consequences of this adverse trend for analog design must be understood better.

2.3.2 NOISE

Currently available deep submicron technologies are mainly developed for digital applications. Noise characteristics are modeled with limited accuracy. A preliminary but promising measurement of a noise figure for an NMOS and PMOS devices is shown below.

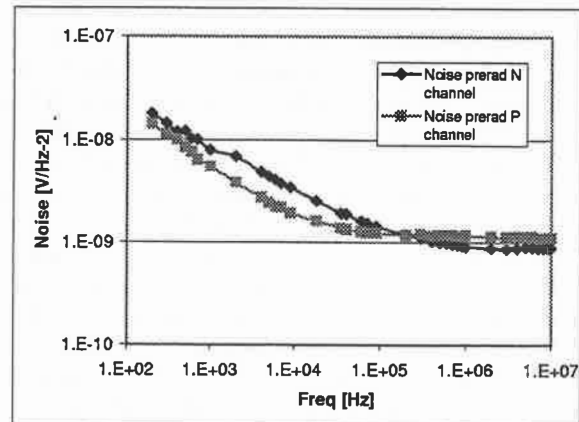

Figure 4 Noise measurement for NMOS and PMOS devices.

2.3.3 Single Event Upset (SEU)

The loss of data bit (configuration, calibration words) in a control circuit might be hard to detect in front-end chips. Scaling of supply voltages and gate capacitance makes deep submicron intrinsically more susceptible to SEU than previous technologies. Solutions to this problem are essentially of three types:

- Layout level solution: The capacitance of critical nodes can be increased; this has been done with the enclosed transistor layouts and is partially effective. This technique has a unacceptable high penalty if applied blindly on a standard cell library (high node capacitances give low speed and high power consumption), and one would force the provision of different versions of the same storage cell with different upset strengths.
- Circuit level solutions: redundant storage cells can be designed with a variety of alternatives. This solution is applied also in commercial gate array libraries and can be very effective, provided one can afford the extra area.
- System level solutions: safe circuits can be obtained using normal cells by introducing system level redundancy, such as parity and/or error detection and correction in data paths and state machines controlling the correctness of their states (one-hot etc.). In our opinion this is the best technique because it leaves essentially to the designer the freedom to select his/her optimal point in the redundancy / robustness space.

An LET threshold of 15 MeV*cm^2/mg has been measured recently on flip-flops implemented on a quarter micron technology with a conventional (non-redundant, static) architecture (Ref. [8]) indicating a good intrinsic robustness. These data have to be interpreted taking into account the energy spectrum of the LHC background radiation, before any conclusive result can be drawn.

Until now all the modeling and measurement efforts were concentrated on understanding the characteristics of storage cells. It is not excluded that ionizing particles could hit logic cells and/or clock trees at the wrong time and produce unwanted glitches. To the best of our knowledge, no systematic study of such effects in deep submicron has been performed until now.

2.4 *Is Yield an Issue ?*

Industry's standard yield for digital circuits requires today a defect density well below 0.2 def/cm^2. Analog yield can be a strong function of circuit design (if the designer does not take into account process spread appropriately), and its optimization requires an intimate knowledge of the process technology used. This is not easily available outside the foundry. To avoid expensive trimming of pre-packaged parts or low yield, designers will have to include circuitry to self-calibrate their ICs using a suitable external or internal reference.

To perceive the approximate scale of the problem, an 8" wafer can yield more than 500 good chips of ~40 mm^2. Such a chip may contain 32 measurement channels and be needed in 2-300,000 channels in a typical medium scale HEP detector. Development effort may run easily to 4-6 man·years.

By using a high volume fab-line, the cost of even a large size HEP ASIC project is therefore clearly dominated by R&D costs. This reality must be understood at the managerial level to avoid unwelcome surprises.

2.5 *Technology Lifetime: What about 0.18 microns ?*

Industry is moving towards 0.18 µm CMOS at a very fast pace [12]. This move will be accompanied by another major step, i.e. the introduction of 300 mm wafers. While it is reasonable to assume that the good radiation resistance characteristics will be maintained in this generation, the introduction of the larger wafers will require completely new handling and testing equipment, and this might indeed be late for LHC. In addition, the larger wafer size demands an even larger production volume to become economically attractive to the fabs.

This generation might also see the appearance of new low-K dielectric materials to reduce wiring capacitances; the resistance of such new materials to radiation will have to be studied carefully.

3 Key Challenges

The key technical and economical challenges associated with the introduction of deep submicron technologies in HEP are briefly discussed below.

3.1 *Design Remapping*

Circuit topologies for analog applications can not always be remapped directly onto new deep submicron technologies. The reduction of V_{DD} with almost constant V_t and the constraint imposed by requiring enclosed NMOS devices may require a total or partial circuit redesign. In addition, the augmented number of available metals can be used for improving density or signal quality.

The W/L parameter in enclosed NMOS devices is not any longer free, making some current mirrors painful to implement.

3.2 *Tools and Design Methodology*

A typical coupling capacitance of a metal wire in a submicron technology may approach 0.2 fF/µm when adding all parasitics from neighbor wires. This compares with perhaps 15-30 fF of gate input capacitance (these might have been 0.1 fF/µm and ~100 fF respectively in a 0.6 µm technology). Metal interconnections are therefore becoming the dominating delay between logic cells.

Presently available synthesis tools are essentially based on logic optimization, with an option on optimizing for speed or for area. Delays models are associated with gates and these are the principal elements that determine path delays. Deep submicron technologies move the

focus from gates to wires, which unfortunately is a strong function of the number of metals and of the final placement of the ASIC. The recent introduction of copper as interconnection metal for VLSI tends to alleviate this adverse trend moderately.
A much stronger contribution to design optimization needs to be provided by the CAE tools. The simple linear flow from early design synthesis, followed by place and route and capacitance back-annotation becomes complicated by requiring a good back annotation estimation to be known at an early phase of the design. High performance designs will depend heavily on the availability of such tools. Fortunately ASICs for HEP rarely have time critical paths (typical operating speed is < 100 MHz), and synthesis may still proceed along the traditional path.

Tools are also needed for other functions, such as automatic metal filling for planarization purposes. Such tools can be programmed rather easily for digital applications (an application can be seen in [13]), but can be rather difficult for analog designs, because of the extra couplings such floating layers may introduce.

3.2.1 Analog models

The accuracy of analog models for deep submicron technologies has been examined in detail in [14] and [15]. In addition to the usual parameters studied in these papers, models for HEP should include the device degradation due to radiation. Fortunately these effects are quite limited in deep submicron, but a detailed study of these effects is still lacking.

3.3 Libraries

For several years the trend in the semiconductor market has clearly been oriented towards a concentration of foundries in large companies, while many design houses are becoming fab-less.

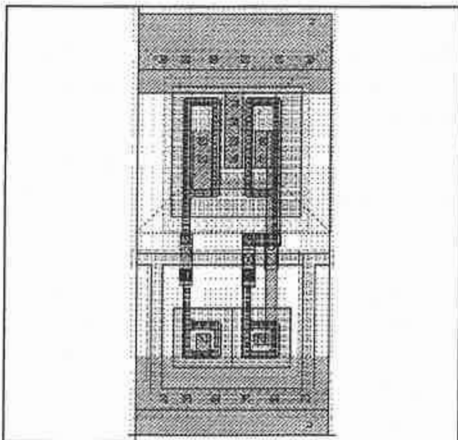

Figure 5 Example of NAND2 gate drawn with radiation resistant layout rules. Notice that the two NMOS devices are fully latchup protected in their own well.

In addition, an increasing number of silicon foundries and their customers are becoming dependent on a few specialized companies providing digital libraries for deep submicron. Today a number of portable libraries are available from several sources, and their cost can be a significant fraction of an HEP ASIC project.
What makes these libraries expensive and difficult to build is not the logic circuit themselves, but the difficulty in providing accurate timing models when long metal interconnects are present.
A special library designed with radiation resistant rules [16] has been developed recently to satisfy the request for total dose tolerance, as well as latchup immunity and single event upset. This library uses very conservative design rules and is therefore far from optimal for a native quarter micron technology; nevertheless it can still be considerably denser (~ 8 times) than in a generic 0.8 micron technology. In addition, the possibility of using more than two metals for signal routing, makes routing channels redundant and another 40% area can probably be gained.
The typical power consumption of a library cell when powered at 2 V is ~0.15 μW/gate*MHz, a reduction of more than one order of magnitude with respect to a 5 V 0.8 μm technology.

3.4 Testing and Design Verification

Testing in deep submicron is in principle no different from testing of previous technologies, apart from potentially having to observe more nodes, given the higher design density offered in new technologies. Nevertheless this aspect of design has been left relatively uncovered until now in our community and will require much more attention in the future.
The testing issue is of paramount importance to guarantee an acceptable level of reliability for modules that can not be accessed – sometimes for many months – such as the front-end cards installed in LHC experiments.
Traditional testing techniques, based on ad-hoc test boards, must be replaced or enhanced by parametric testers, which can exercise a circuit under a whole range of supply, timing and temperature conditions, thus ensuring robustness over a wide range of operating conditions. Self-calibration techniques must also be adopted at the circuit level, to have ASICs adapt themselves to new operating conditions, after – for instance – irradiation induced damage has occurred [17].
Testing can also represent a significant part of the ASIC cost, especially when this aspect is neglected at design time. The operation of a typical integrated circuit tester can cost of the order of several dollars per minute, with an investment ranging in the 5-10,000 US$ per channel for a production tester and about one third as much for a design verification tester. In addition, no 'standard' mixed-signal tester exists, and each measurement con-

figuration may require and ad-hoc setup, demanding a large programming effort.
JTAG is a well established standard in the digital test domain, but testing of mixed signal ASICs requires much more designer ingenuity to shorten expensive tester time.
Finally, while digital test vectors translation is painful, but part of many design kits, analog 'test-vectors' are not easily transferable, and each measurement requires a specific configuration. Analog ATPG is not a well defined concept either, making analog testing more expensive than digital testing.
ASICs designed in HEP are largely surpassed by commercial integrated circuits with respect to performance of single channels, but the integration of many analog channels at low power in a single chip is still unique to particle physics data acquisition systems. Pulse electronics and analog memories as used in HEP ASICs are not always susceptible to standard testing techniques used, for instance, in commercial RF equipment, such as FFT and spectral analysis. Analog memories would require a per-cell calibration which may need thousand of input pulses to be generated and therefore long testing time might be required.

3.5 ECONOMIC ASPECTS

The global semiconductor market amounts to about 130B$ for 1998 and is growing at about 15% annually. Many fabs worldwide are capable of processing in excess of 10,000 8" wafers per week. Any order coming for LHC electronics can only be of limited interest for such a foundry, especially considering that the investor has to amortize 1-2 B$ to recover the cost of the foundry itself.
Economic factors whose control is totally outside the influence of the HEP community have to be clearly understood through proper cost assessment to minimize the risks and lower the costs. While the investment in microelectronics seems huge from a physicist perspective, our business is next to negligible for any modern high-volume silicon foundry, therefore demanding a much better coordinated approach to the foundry that englobes all collaborating HEP Institutes. The economic trade-offs between a generic high-volume, low cost technology and a special high-quality, expensive one should also be evaluated against the cost of design development.

4 CONCLUSION

Deep submicron technology may allow the construction of ASICs for experiments of the LHC generation with good radiation tolerance and low manufacturing costs. In addition, power consumption reduction of up to an order of magnitude in digital chips can also substantially reduce and simplify the cost of infrastructure equipment on detectors. The total costs of such devices must still be accounted properly by taking into account development and testing costs.
Today's microelectronics industry is chronically much weaker in providing good design tools for leading edge technologies and a large collaborative effort between HEP laboratories is necessary to make this technology generally available, especially for mixed-signal ASICs.

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6 REFERENCES.

[1] G. Anelli et al., '*Total Dose behavior of submicron and deep-submicron CMOS technologies*', in Proceedings of the Third Workshop on Electronics for LHC Experiments, London, September 22-27, 1997
[2] M. Bohr et al., '*Technology for Advanced High-Performance Microprocessors*' in Transactions on Electron Devices, March 1998, p.620
[3] Semiconductor Industry Association, '*The National Technology Roadmap for Semiconductors*', Semiconductor Industry Association, 1997 Edition
[4] Y. Oowaki et al., '*A Sub-0.1 mm Circuit Design with Substrate over Biasing*', in Proceeding of the 1998 IEEE International Solid State Circuit Conference, p. 88
[5] T. Masuda et al., '*40 Gb/s Analog IC Chipset for Optical Receiver using SiGe HBTs*', in Proceedings of the 1998 IEEE International Solid State Circuit Conference, February 1998, p. 314
[6] A. Dingwall et al. '*C2L: A New High Speed High-Density Bulk CMOS Technology*', IEEE Journal of Solid State Circuits, August 1977, p. 344
[7] M. Walters, A. Reisman, '*The distribution of radiation-induced charged defects and neutral electron traps in SiO_2 and the threshold voltage shift dependence on oxide thickness*', Journal of Applied Physics, March 1990, p. 2992
[8] F. Faccio et al., '*Total Dose and Single Event Upset Measurements of Test Structures in a Deep-Submicron Technology*', in the Proceedings of Fourth Workshop on Electronics for LHC Experiments, Rome, September 21-25, 1998
[9] G. Sai-Halasz et al. '*CMOS Scaling into the 21st Century: 0.1 μm and beyond*', IBM Journal or R&D, January 1995, p. 245
[10] A. Giraldo, PhD Thesis at the University of Padova-Italy, to be published.
[11] J. Chen et al., '*Statistical Circuit Characterization for Deep-Submicron CMOS Design*', in Proceedings of the 1998 IEEE International Solid State Circuit Conference, February 1998, p. 90

[12] Hiroshi Iwai, ' *CMOS – Year 2010 and beyond: from Technological side*', Proceedings of the 1998 IEEE Custom Integrated Circuit Conference, p.141
[13] P. E. Gronowski et al., '*High Performance Microprocessor Design*', in IEEE Journal of Solid State Circuits, May 1998, p. 676
[14] B. Razavi, ' *CMOS Technology Characterization for Analog and RF Design*', in Proceedings of the IEEE Custom Integrated Circuit Conference 1998, p. 23
[15] Q. Huang et al., '*The Impact of Scaling Down to Deep Submicron on CMOS RF Circuits*', IEEE Journal of Solid State Circuits, July 1998, p. 1023
[16] K. Kloukinas et al.. '*Development of a Radiation Tolerant 2.0 V standard cell library using a commercial deep submicron CMOS technology for the LHC experiment*', in the Proceedings of The Fourth Workshop on Electronics for LHC Experiments, Rome, September 21-25, 1998
[17] P. Placidi et al. '*A PLL-Delay ASIC for Clock recovery and trigger distribution in the CMS tracker*', in Proceedings of the Third Workshop on Electronics for LHC Experiments, London, September 22-27, 1997