3-2-1 Phase D-Cap+™ Step-Down Driverless Controller for Tegra™ CPUs with Serial VID Control and DVFS

Check for Samples: TPS51632

FEATURES

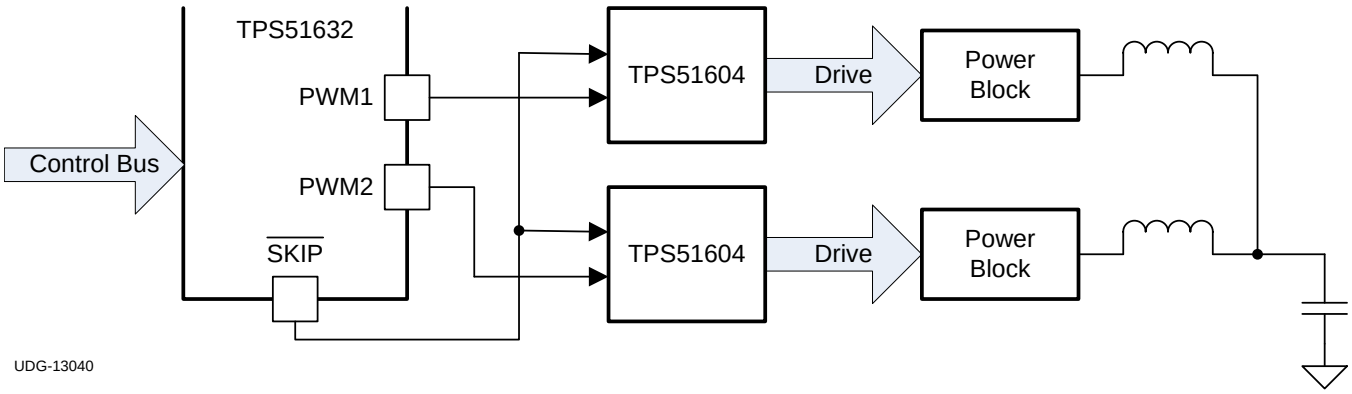
- **Selectable Phase Count: (3, 2, or 1)**
- **Dynamic Voltage and Frequency Scaling (DVFS) Digital Interface**
- **I^2C Interface for VID Control and Telemetry with Eight Device Addresses**
- **D-CAP+™ Control for Fast Transient Response**
- **Dynamic Phase Add and Drop Operation**
- **Switching Frequency: 300 kHz to 1 MHz**
- **Digital Current Monitor**
- **7-Bit DAC Output Range: 0.50-V to 1.52-V**
- **Optimized Efficiency at Light and Heavy Loads**
- **V_{CORE} Overshoot Reduction (OSR™)**
- **Accurate, Adjustable Voltage Positioning or Zero Slope Load-Line**
- **Patented AutoBalance™ Phase Balancing**
- **Selectable 8-Level Current Limit**
- **2.5-V to 24-V Conversion Voltage Range**
- **Small 4-mm x 4-mm, 32-Pin, QFN PowerPAD Package**

DESCRIPTION

The TPS51632 is a driverless step down controller with serial control. Advanced features such as D-CAP+™ architecture with overlapping pulse support and OSR overshoot reduction provide fast transient response, lowest output capacitance and high efficiency. The TPS51632 supports both I^2C and DVFS interfaces for dynamic control of the output voltage and current monitor telemetry. It also has dynamic phase add and drop control and enters single-phase, discontinuous-current-mode operation to maximize light-load efficiency.

The TPS51632 supports Tegra™ requirements for PGOOD interrupts for MaxVID violations and *near OCP* conditions. This interrupt behavior is programmable via I^2C. Adjustable control of V_{CORE} slew rate and voltage positioning round out the features. The TPS51604 driver is designed specifically for this generation of controllers. The TPS51632 is packaged in a space saving, thermally enhanced 32-pin QFN and is rated to operate at a range between –10°C and 105°C.

SIMPLIFIED APPLICATION DIAGRAM



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)(2)

T_A	PACKAGE	ORDERABLE NUMBER	PINS	OUTPUT SUPPLY	MINIMUM QUANTITY
–40℃ to 105℃	Plastic Quad Flat Pack (QFN)	TPS51632RSMT	32	Small tape and reel	250
		TPS51632RSMR		Large tape and ree	3000

(1) For the most current package and ordering information, see the *Package Option Addendum* at the end of this document, or visit the TI website at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input Voltage	VDD	0.0	3.5	V
	PWM3, PWM2, PWM1, SKIP	0.0	5	
	VBAT	0.0	28	
	V5A	0.0	5.5	
	O-USR, FREQ-P, B-RAMP, OCP-I, IMON, VREF	0.0	1.7	
	COMP, DROOP	0.0	3.5	
	GFB	-0.1	0.1	
	VFB, CSP1, CSP2, CSP3, CSN1, CSN2, CSN3	0.0	1.6	
	V1P8	0.0	2.0	
	SLEWA	0.1	1.7	
	EN, PWM_CL, SDA, PWM_DT, SCL	0.0	1.8	
Output Voltage	PGOOD	0.0	3.3	V
Storage temperature range, T_{stg}		–55	150	°C
Junction temperature range, T_J		–40	150	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input Voltage	VDD, O-USR, B-RAMP,OCP-I, IMON, VREF, VFB, CSP1, CSP2, CSP3, CSN1, CSN2, CSN3, V1P8, PWM_CL, SDA, PWM_DT, SCL	-0.3	3.6	V
	PWM3, PWM2, PWM1, $\overline{SKIP}$	-0.3	3	
	VBAT	-0.3	36	
	V5A, FREQ-P, COMP, DROOP, SLEWA, EN,	-0.3	6	
	GFB	-0.2	0.2	
Output Voltage	PGOOD	-0.3	3.6	V
Operating free-air temperature, T_A		–10	105	°C

THERMAL INFORMATION

THERMAL METRIC(1)		TPS51632 RSM (QFN) 32 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	37.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	31.9	
θ_{JB}	Junction-to-board thermal resistance(4)	8.1	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.4	
ψ_{JB}	Junction-to-board characterization parameter(6)	7.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	2.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS

over recommended free-air temperature range, 4.5 V ≤ V_{V5A} ≤ 5.5 V, 3.0 V ≤ V_{VDD} ≤ 3.6 V, V_{GFB} = GND, V_{VFB} = V_{CORE} (unless otherwise noted).

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY: CURRENTS, UVLO AND POWER-ON-RESET						
I_{V5-3P}	V5A supply current, 3-phase	V_{VDAC} < V_{VFB} < (V_{VDAC} + 100 mV), EN= 'HI'		3.6	6.0	mA
I_{VDD-3P}	VDD supply current, 3-phase	V_{VDAC} < V_{VFB} < (V_{VDAC} + 100 mV) , EN= 'HI'; digital buses idle		0.2	0.8	
I_{V5-1P}	V5A supply current, 1-phase	VDAC < VFB < (V_{VDAC} + 100 mV) EN='HI'		3.5	6.0	
I_{VDD-1P}	VDD supply current, 1-phase	VDAC < VFB < (V_{VDAC} + 100 mV), EN='HI'; Digital buses idle		0.2	0.8	
I_{V5STBY}	V5A standby current	EN= 'LO'		125	200	µA
$I_{VDDSTBY}$	VDD standby current	EN= 'LO'		23	40	
$I_{VDD-1P8}$	V1P8 supply current	All conditions; Digital buses idle		1.7	5.0	
V_{UVLOH}	V5A UVLO 'OK' threshold	V_{VFB} < 200 mV. Ramp up; V_{VDD} > 3 V; EN='HI'; Switching begins.	4.25	4.4	4.5	V
V_{UVLOL}	V5A UVLO fault threshold	Ramp down; EN= 'HI'; V_{VDD} > 3 V; V_{VFB} = 100 mV. Restart if 5-V falls below V_{POR} then rises > V_{UVLOH}, or EN is toggled w/ V_{V5A} > V_{UVLOH}	4.00	4.2	4.3	
V_{POR}	V5A fault latch reset threshold	Ramp down. EN='HI'; V_{VDD} > 3 V. Can restart if 5-V rises to V_{UVLOH} and no other faults present.	1.2	1.9	2.5	
V_{3UVLOH}	VDD UVLO 'OK' threshold	V_{VFB} < 200 mV. Ramp up; V_{V5A} > 4.5 V; EN='HI'; Switching begins.	2.5	2.8	3.0	
V_{3UVLOL}	Fault threshold	Ramp down; EN= 'HI'; V5A > 4.5V; VFB = 100 mV. Restart if 5V dips below VPOR then rises > V_{UVLOH} or EN is toggled with 5 V > V_{UVLOH}	2.4	2.6	2.8	
V_{POR}	VDD fault latch	Ramp Down. EN='HI'; V5A > 4.5V. Can restart if 5-V goes up to V_{UVLOH} and no other faults present.	1.2	1.9	2.5	
$V_{1P8UVLOH}$	V1P8 UVLO OK	Ramp up; EN= 'HI'; V5A > 4.5V; VFB = 100mV.	1.4	1.5	1.6	
$V_{1P8UVLOL}$	V1P8 UVLO falling	Ramp down; EN= 'HI'; V5A > 4.5V; VFB = 100mV.	1.3	1.4	1.5	
REFERENCES: DAC, VREF, VFB DISCHARGE						
V_{VIDSTP}	VID step size	Change VID0 HI to LO to HI		10		mV
V_{DAC1}	VFB tolerance, No load active	1.36 V ≤ V_{VFB} ≤ 1.52 V, I_{OUT} = 0 A	–9		9	
V_{DAC2}	VFB tolerance No load medium V	1.0 V ≤ V_{VFB} ≤ 1.35 V; I_{OUT} = 0 A	–8		8	
		0.5 V ≤ V_{VFB} ≤ 0.99 V; I_{OUT} = 0 A	-7		7	
V_{VREF}	VREF output	VREF output 4.5 V ≤ V_{V5A} ≤ 5.5 V, I_{VREF} = 0 A	1.66	1.700	1.74	V
$V_{VREFSRC}$	VREF output source	0 A ≤ I_{REF} ≤ 500 µA, HP-2	–4	-3		mV
$V_{VREFSNK}$	VREF output sink	–500 A ≤ I_{REF} ≤ 0 A, HP-2		3	4	
V_{VBOOT}	Internal VFB initial boot voltage	Initial DAC boot voltage	1.02	1.10	1.18	V
BOOT VOLTAGE AND RAMP SETTINGS						
V_{RAMP}	Compensation ramp	R_{RAMP} = 30 kΩ		60		mV
		R_{RAMP} = 56 kΩ		120		
		R_{RAMP} = 100 kΩ		160		
		R_{RAMP} ≥150 kΩ; use internal ramp		40		
VOLTAGE SENSE: VFB AND GFB						
R_{VFB}	VFB/GFB Input resistance	Not in fault, disable or UVLO, V_{VFB}= V_{DAC}= 1.5 V, V_{GFB} = 0 V, measure from VFB to GFB	1			MΩ
V_{DELGND}	GFB Differential	GND to GFB		±100		mV
CURRENT MONITOR						
VAL_{ADC}	IMON ADC output	∑ΔCS = 0 mV, A_{IMON} = 3.867		00h		
		∑ΔCS = 1.5 mV, A_{IMON} = 3.867		19h		
		∑ΔCS = 7.5 mV, A_{IMON} = 3.867		80h		
		∑ΔCS = 15 mV, A_{IMON} = 3.867		FFh		
LR_{IMON}	IMON linear range	Each phase, CSPx – CSNx	50			mV

ELECTRICAL CHARACTERISTICS (continued)

over recommended free-air temperature range, 4.5 V ≤ V_{V5A} ≤ 5.5 V, 3.0 V ≤ V_{VDD} ≤ 3.6 V, V_{GFB} = GND, V_{VFB} = V_{CORE} (unless otherwise noted).

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT SENSE: OVER CURRENT PROTECTION, PHASE ADD AND DROP, AND PHASE BALANCE						
V_{OCPP}	OCP voltage (valley current limit)	R_{OCP-I} = 39 kΩ	15.4	19.5	23.0	mV
		R_{OCP-I} = 56 kΩ	21.3	25.4	29.0	
		R_{OCP-I} = 75 kΩ	28.4	32.5	36.2	
		R_{OCP-I} = 100 kΩ	36.3	40.5	44.0	
		R_{OCP-I} = 150 kΩ	45.0	49.3	53.0	
I_{AD23}	Phase add	Valley current, % of OCP value, mode changes from 2-phase CCM to 3-phase CCM		25%		
I_{AD12}	Phase add	Valley current, % of OCP value, mode changes from 1-phase DCM to 2-phase CCM		10%		
I_{AD32}	Phase drop	Valley current, % of OCP value, mode changes from 3-phase CCM to 2-phase CCM		15%		
I_{AD21}	Phase drop	Valley current, % of OCP value, mode changes from 2-phase CCM to 1-phase DCM		7%		
I_{CS}	CS pin input bias current	CSPx and CSNx	–500	0.2	500	nA
A_{V-EA}	Error amplifier totalvoltage gain(1)	VFB to DROOP	80			dB
I_{EA_SR}	Error amplifier source current	I_{DROOP}, V_{VFB} = V_{DAC} + 50 mV, R_{COMP} = 1 kΩ		1		mA
I_{EA_SK}	Error amplifier sink current	I_{DROOP}, V_{VFB} = V_{DAC} – 50mV, R_{COMP} = 1 kΩ		–1		
I_{BAL_TOL}	Internal current share tolerance	V_{DAC} = 1.7 0V, V_{CSP1} – V_{CSN1} = V_{CSP2} –V_{CSN2} = V_{CSP3} – V_{CSN3} = V_{OCPP_MIN}	–3%		+3%	
A_{CSINT}	Internal current sense gain	Gain from CSPx – CSNx to PWM comparator, $R_{\overline{SKIP}}$ = Open	5.8	6.0	6.2	V/V
TIMERS: SLEW RATE, ADDR, SLEEP EXIT, ON-TIME AND I/O TIMING						
$t_{START-CB}$	Cold boot time	V_{BOOT} > 0V , EN = high, time from UVLO to VOUT ramp, C_{REF} = 0.33 µF			1.2	ms
t_{STBY-E}	STBY exit time	Time from EN assertion until PGOOD goes high. V_{VID} = 1.28 V, R_{SLEW} = 39 kΩ			250	µs
SL_{SET}	Slew rate setting for VID change	R_{SLEW} = 39 kΩ	24			mV/µs
		R_{SLEW} = 54 kΩ	30			
		R_{SLEW} = 75 kΩ	36			
		R_{SLEW} = 100 kΩ	42			
		R_{SLEW} = 150 kΩ	48			
SL_{START}	Slew rate setting for start-up	EN goes high, R_{SLEW} = 39 kΩ	12			
ADDR	Address Setting 3 LSB of I^2C Address	V_{SLEWA} ≤ 0.30 V (Addr = 100 0xxx)		000b		
		0.75 V ≤ V_{SLEWA} ≤ 0.85 V		011b		
		1.15 V ≤ V_{SLEWA} ≤ 1.25 V		101b		
$t_{PGDDGLTO}$	PGOOD deglitchtime	Time from VFB out of 250 mV VDAC boundary to PGOOD low.		1		µs
$t_{PGDDGLTU}$	PGOOD deglitch time	Time from VFB out of -300 mV VDAC boundary to PGOOD low.		31		
I_{PGDLO}	PGOOD current warning value	Percentage of OCP value		70%		
R_{VBAT}	VBAT resistance	EN= HI		550		kΩ
		EN= LOW or STBY	10			MΩ
t_{ON}	On-time	R_{CF} = 24 kΩ, V_{BAT}= 12 V, V_{VFB} = 1 V (400 kΩ)		208		ns
		R_{CF} = 39 kΩ, V_{BAT}= 12 V, V_{VFB} = 1 V (600 kΩ)		139		
		R_{CF} = 75 kΩ, V_{BAT}= 12 V, V_{VFB} = 1 V (800 kΩ)		104		
		R_{CF} = 150 kΩ, V_{BAT}= 12 V, V_{VFB} = 1 V (1 MkΩ)		83		

(1) Specified by design. Not production tested.

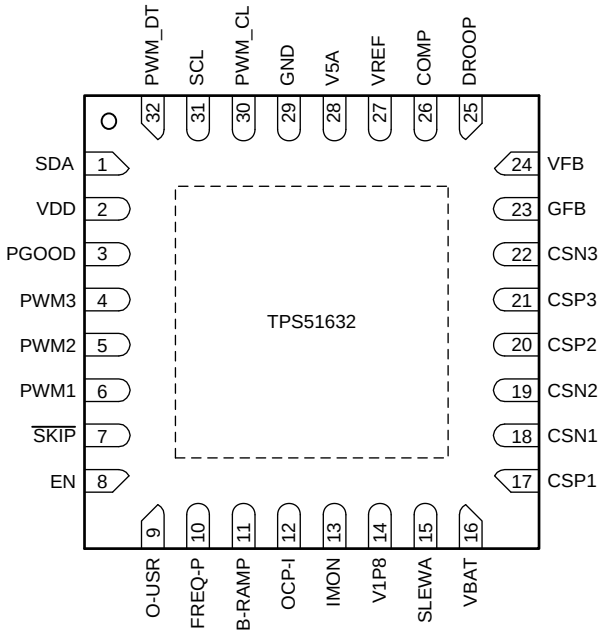
ELECTRICAL CHARACTERISTICS (continued)

over recommended free-air temperature range, 4.5 V ≤ V_{V5A} ≤ 5.5 V, 3.0 V ≤ V_{VDD} ≤ 3.6 V, V_{GFB} = GND, V_{VFB} = V_{CORE} (unless otherwise noted).

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V_{DP_OFF}	Voltage to disable dynamic phase add/drop	Voltage at FREQ-P at start-up	0.70			V
V_{DP_ON}	Voltage to enable dynamic phase add/drop	Voltage at FREQ-P at start-up			0.40	
V_{DP_HYS}	Hysteresis voltage of phase add/drop circuit	Voltage at FREQ-P at start-up		80		mV
t_{OFF_MIN}	Controller minimum OFF time	Fixed Value	20			ns
t_{ON_MIN}	Controller minimum ON time	R_{CF} = 150 kΩ, V_{BAT}=20 V, V_{VFB} = 0 V	20			
t_{VCCVID}	VID change to VFB change(2)	ACK of VID change command to start of voltage ramp			1	µs
R_{SFTSTP}	Soft-stop transistor resistance	Connected to CSN1		100	200	Ω
PROTECTION: OVP, UVP, PGOOD AND THERMAL SHUTDOWN						
V_{OVPH}	Fixed OVP voltage	V_{CSN1} or V_{GCSN} > V_{OVPH} for 1 µs, DRVL→ ON	1.60	1.70	1.80	V
V_{PGDH}	PGOOD high threshold	Measured at the VFB pin w/r/t VID code, device latches OFF	190		245	mV
V_{PGDL}	PGOOD low threshold	Measured at the VFB pin w/r/t VID code, device latches OFF	-348		-280	
t_{PG2}	PGOOD low after enable goes low	Low state time after EN goes low.	225	250	275	µs
PWM AND $\overline{SKIP}$ OUTPUTS: I/O VOLTAGE AND CURRENT						
$V_{P\text{-}S\_L}$	PWMx/$\overline{SKIP}$ - Low	I_{LOAD} = ± 1 mA		0.15	0.3	V
$V_{P\text{-}S\_H}$	PWMx/$\overline{SKIP}$ - High	I_{LOAD} = ± 1 mA	4.2			
$V_{PW\text{-}SKLK}$	PWMx/SKIP# Tri-state	I_{LOAD} = ± 100 µA	1.6	1.7	1.8	
$t_{P\text{-}S\_H\text{-}L}$	PWMx/$\overline{SKIP}$ H-L transition time	C_{LOAD} = 10 pF, I_{LOAD} = ±100µA, 10 to 90%, both edges		7	10	ns
$t_{P\text{-}S\_TRI}$	PWMx/$\overline{SKIP}$ Tri-state transition	C_{LOAD} = 10pF, I_{LOAD} = ±100µA, 10 or 90% to tri-state level, both edges		5	10	
LOGIC INTERFACE: VOLTAGE AND CURRENT						
R_{VRTTL}	Pull-down resistance	SDA, V = 0.31 V	4		15	Ω
R_{VRPG}		PGOOD, V = 0.31 V		36	50	
I_{VRTTLK}	Logic leakage current	SDA, PGOOD, SCL, leakage current, V = 3.3 V, PWM_CL, PWM_DT, V = 1.8 V	-2	0.2	2	µA
V_{IL}	Low-level Input voltage	SCL, SDA, PWM_CL, PWM_DT, $V_{I/O}$ = 1.8 V			0.6	V
V_{IH}	High-level Input voltage		1.2			
I_{ENH}	I/O leakage, EN	Leakage current , V_{EN} = 1.8 V		24	40	µA

(2) Specified by design. Not production tested.

DEVICE INFORMATION



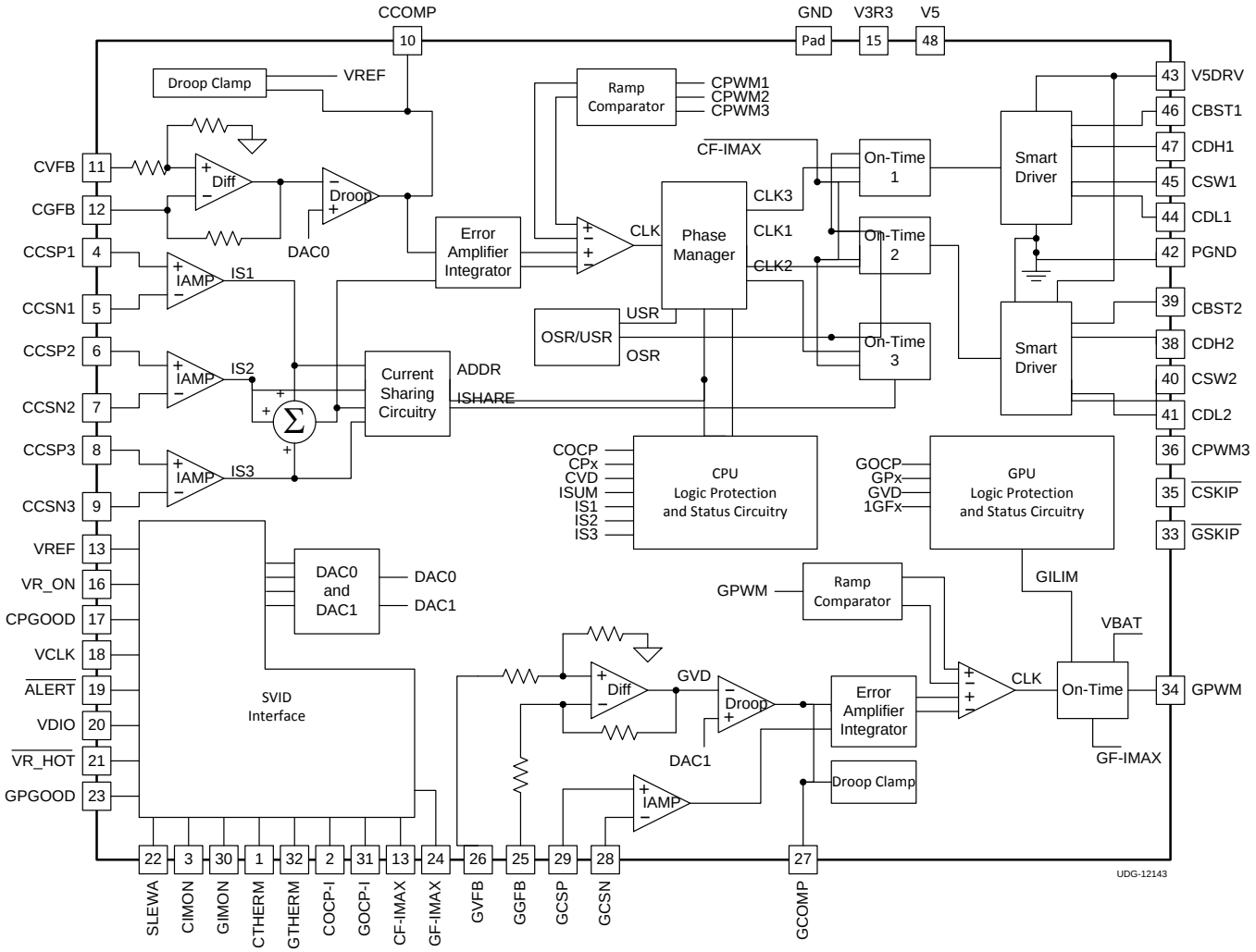
PIN DESCRIPTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
B-RAMP	11	I	Voltage divider to VREF. R to GND sets the ramp setting voltage. The voltage level sets the BOOT voltage. The VBOOT voltage equals the B-RAMP voltage. The RAMP setting can be used to override the factory ramp setting. Both are latched at start-up.
COMP	26	I	Error amplifier summing node. Resistors from VREF to COMP (R_{COMP}) and COMP to DROOP (R_{DROOP}) set the droop gain.
CSP1	17	I	Positive current sense inputs. Connect to the most positive node of current sense resistor or inductor DCR sense network. Tie CSP3, CSP2 or CSP1 (in that order) to 3.3 V to disable the phase.
CSP2	20		
CSP3	21		
CSN1	18	I	Negative current sense inputs. Connect to the most negative node of current sense resistor or inductor DCR sense network. CSN1 has a secondary OVP comparator and includes the soft-stop pull-down transistor.
CSN2	19		
CSN3	22		
DROOP	25	O	Error amplifier output. A resistor pair from VREF to COMP to DROOP sets the droop gain. $A_{DROOP} = 1 + R_{DROOP} / R_{COMP}$.
EN	8	I	Enable; 100-ns de-bounce. Regulator enters low-power mode, but retains start-up settings when brought low.
FREQ-P	10	I	R to GND sets the per phase switching frequency. Add a resistor to VREF to disable dynamic phase add and drop operation.
GFB	23	I	Voltage sense return. Tie to GND on PCB with a 10-Ω resistor to provide feedback when µP is not populated.
GND	29	–	Analog circuit reference; tie to a quiet point on the ground plane.
IMON	13	O	Analog current monitor output. $V_{IMON} = \Sigma V_{ISENSE} \times (1 + R_{IMON}/R_{OCP})$.
OCP-I	12	I/O	Voltage divider to IMON. Resistor ratio sets the IMON gain (see IMON pin). R to GND (R_{OCP}) selects 1 of 8 OCP levels (per phase, latched at start-up).
O-USR	9	I	Voltage divider to VREF. R to GND selects 1 of 7 OSR levels + OFF. Voltage selects 1 of 7 USR levels + OFF.
PGOOD	3	O	Power Good output; Open-drain. PGOOD can be configured to go low when the current reaches 70% of the OCP setting value (= TDC). It can also be configured as an interrupt if DVFS requests a voltage greater than VMAX.

PIN DESCRIPTIONS (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
PWM1	4	O	PWM controls for the external driver; 5-V logic level. Controller forces signal to the tri-state level when needed.
PWM2	5		
PWM3	6		
PWM_CL	30	I	Clock input for DVFS.
PWM_DT	32	I	Data input for DVFS.
SCL	31	I	Serial digital clock line.
SDA	1	I/O	Serial digital I/O line.
$\overline{\text{SKIP}}$	7	O	When high, the driver enters FCCM mode; otherwise, the driver is in DCM mode. Driving the tri-state level on this pin puts the drivers into a low power sleep mode.
SLEWA	15	I	The voltage sets the 3 LSBs of the I^2C address. The resistance to GND selects 1 of 8 slew rates. The start-up slew rate (EN transitions high) is SLEWRATE/2. The ADDRESS and SLEWRATE values are latched at start-up.
V1P8	14	I	Input voltage to power 1.8-V interface logic.
V5A	28	I	5-V power input for analog circuits; connect through resistor to 5-V plane and bypass to GND with ≥1-µF ceramic capacitor
VBAT	16	I	10-kΩ resistor to VBAT provides VBAT information to the on-time circuits for both converters.
VDD	2	I	3.3-V digital power input; bypass to GND with ≥1-µF capacitor.
VFB	24	I	Voltage sense line. Tie directly to VCORE sense point of processor. Tie to VCORE on PCB with a 10-Ω resistor to provide feedback when µP is not populated. The resistance between VFB and GFB is > 1 mΩ
VREF	27	O	1.7-V, 500-µA reference. Bypass to GND with a 0.22-µF ceramic capacitor.
PAD	GND	–	Thermal pad; tie to the ground plane with multiple vias.

FUNCTIONAL BLOCK DIAGRAM



APPLICATION INFORMATION

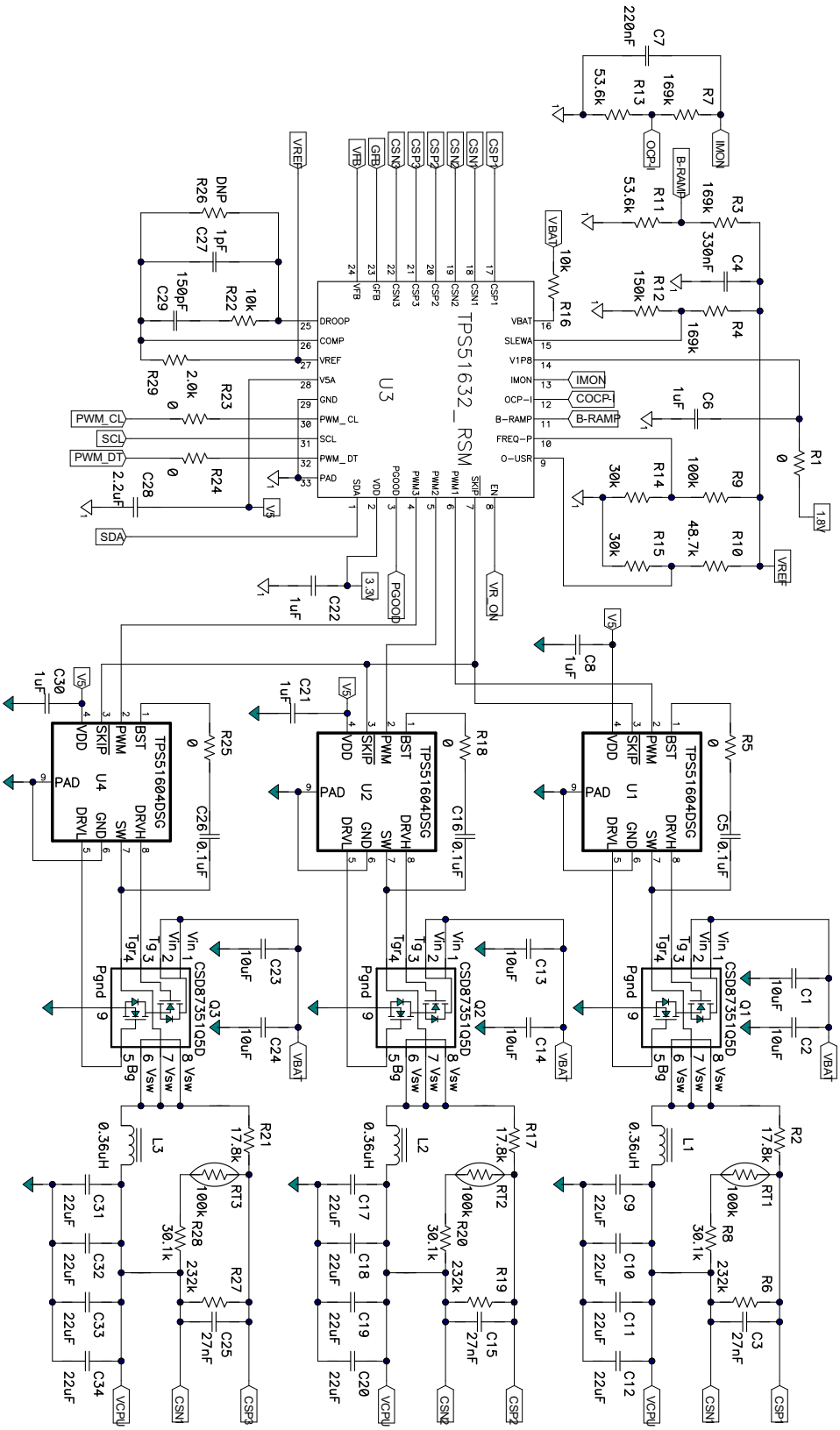


Figure 1. Typical Application Circuit

TYPICAL CHARACTERISTICS (2-Phase Operation)

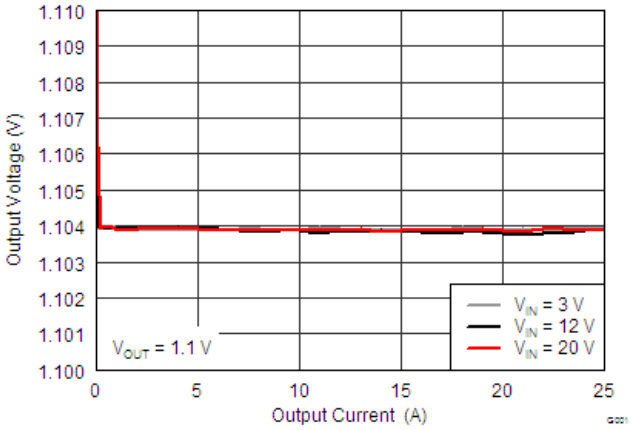


Figure 2. Load Regulation

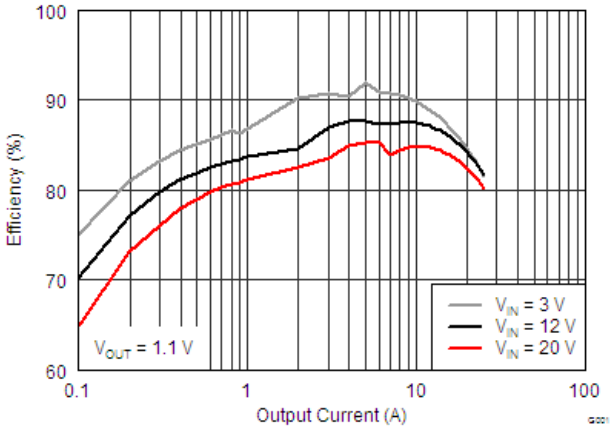


Figure 3. Efficiency vs. Output Current

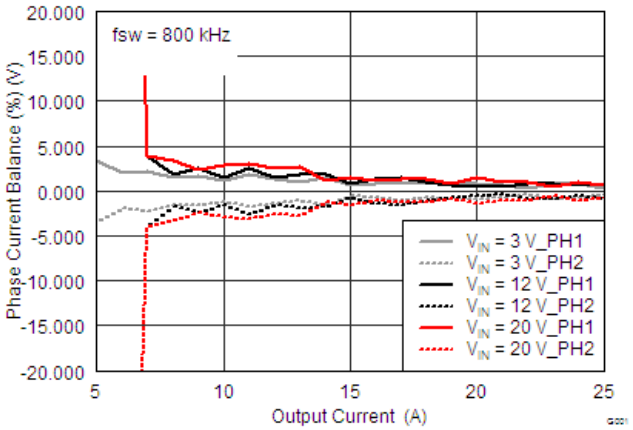


Figure 4. Current Sharing vs. Output Current

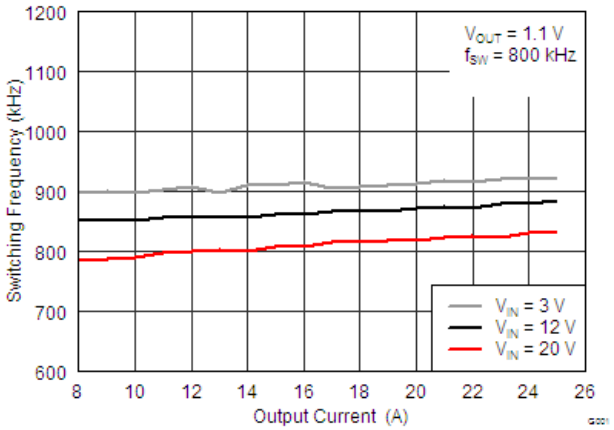


Figure 5. Frequency vs. Output Current

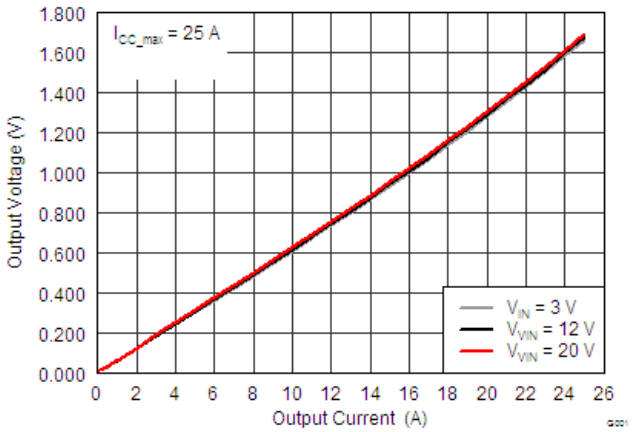


Figure 6. Current Monitor

TYPICAL CHARACTERISTICS (3-Phase Operation)

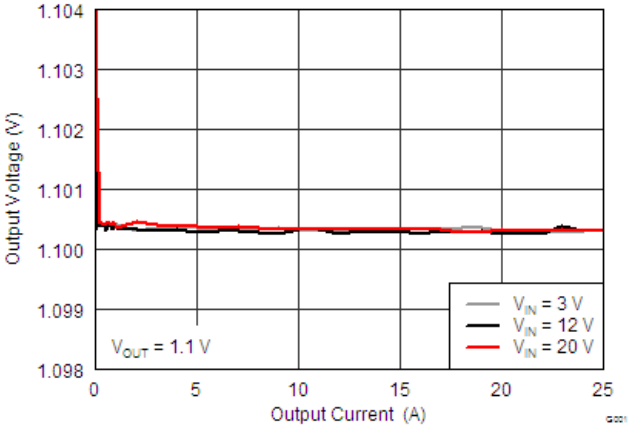


Figure 7. Load Regulation

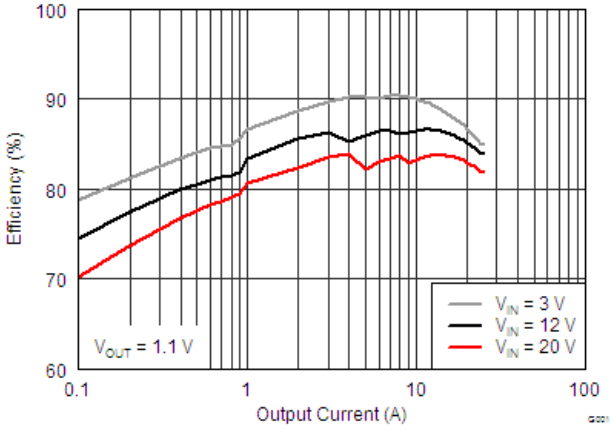


Figure 8. Efficiency vs. Output Current

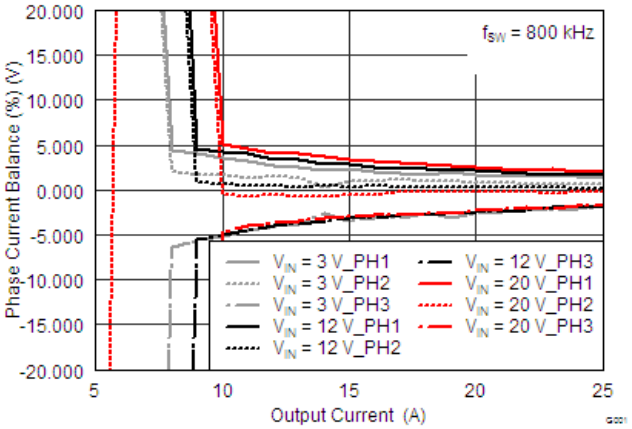


Figure 9. Current Sharing vs. Output Current

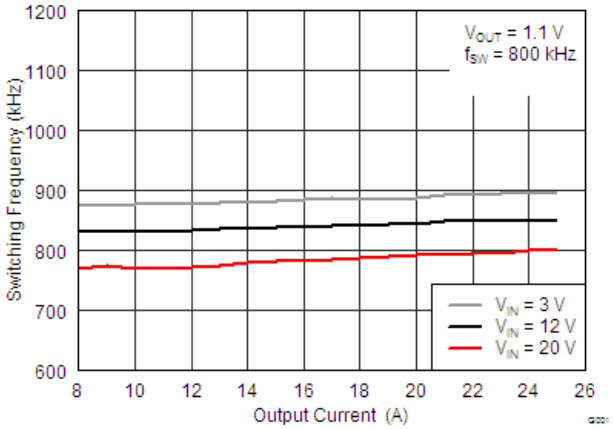


Figure 10. Frequency vs. Output Current

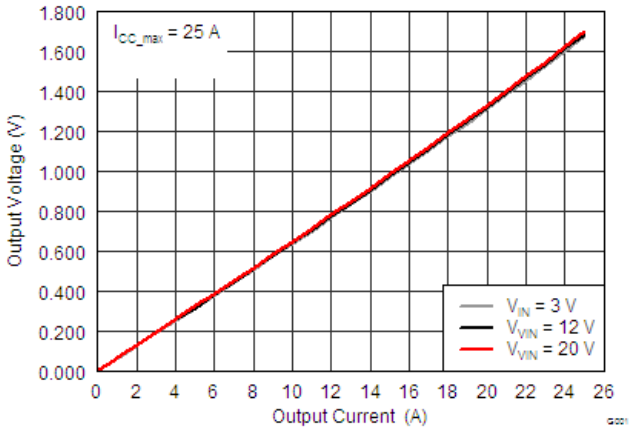


Figure 11. Current Monitor

TYPICAL CHARACTERISTICS

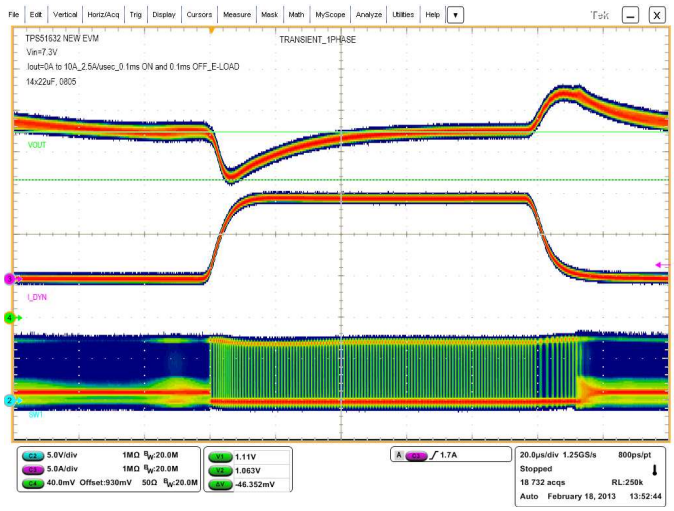


Figure 12. 1-Phase, ΔI = 10 A Transient, ELoad

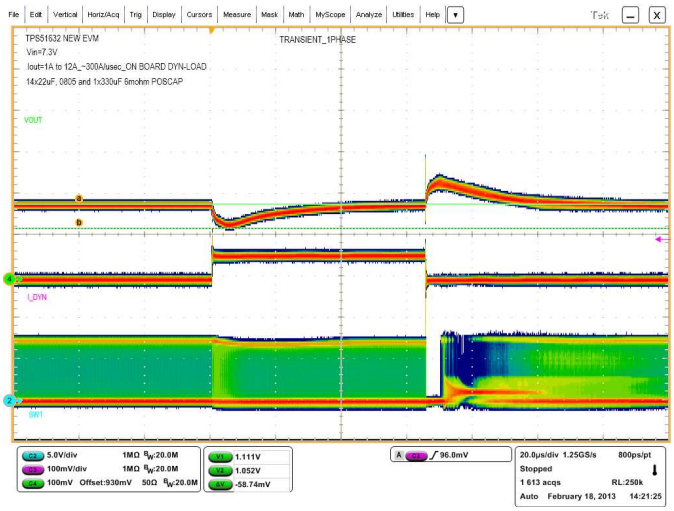


Figure 13. 1-Phase, ΔI = 10 A Transient, On Board Dynamic Load

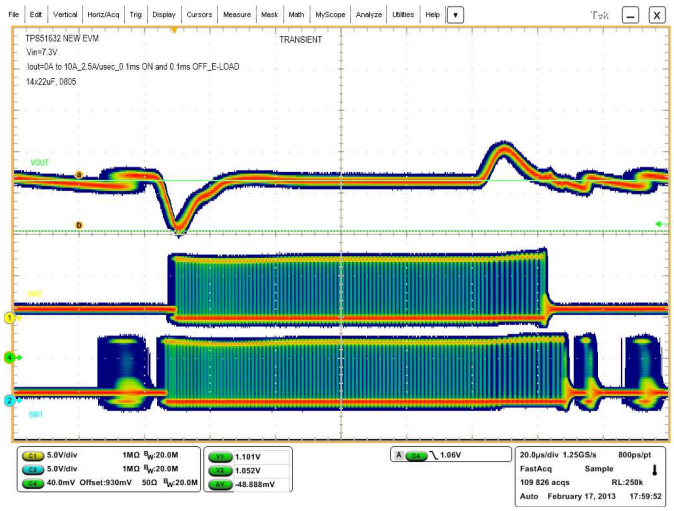


Figure 14. 2-Phase, ΔI = 10 A Transient, ELoad

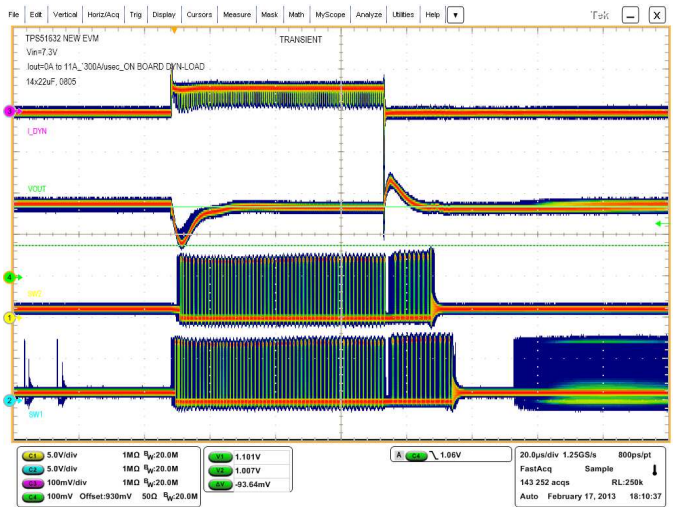


Figure 15. 2-Phase, ΔI = 10 A Transient, On Board Dynamic Load

TYPICAL CHARACTERISTICS (continued)

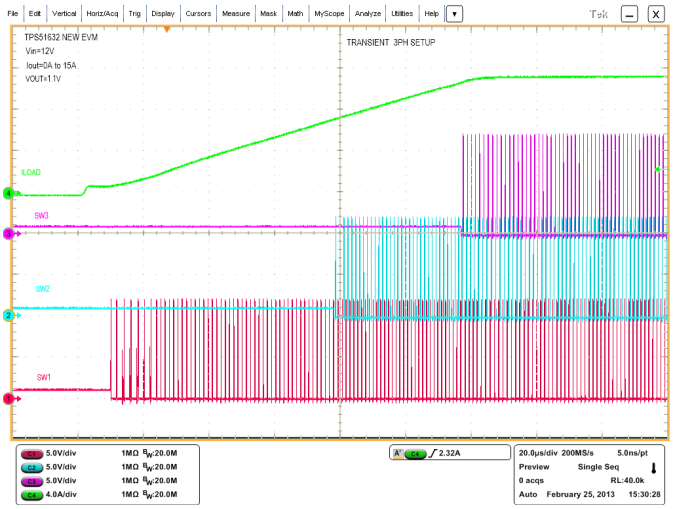


Figure 16. 3-Phase Transient Operation (Phase Add Threshold)

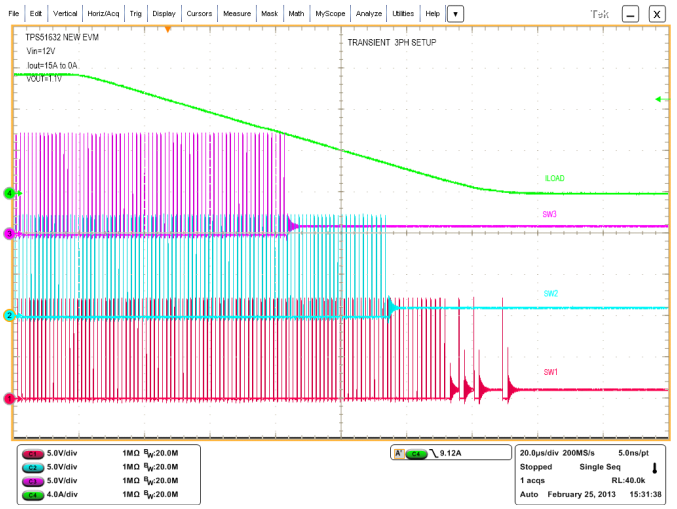


Figure 17. 3-Phase Transient Operation (Phase Drop Threshold)

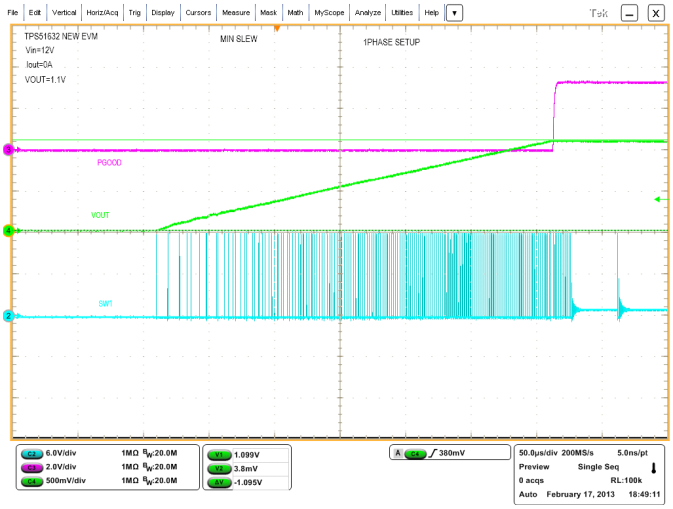


Figure 18. 1-Phase EN Startup

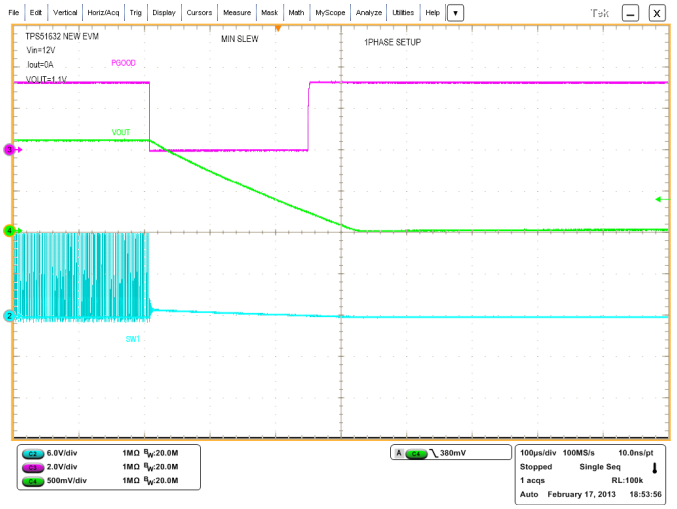


Figure 19. 1-Phase EN Shutdown

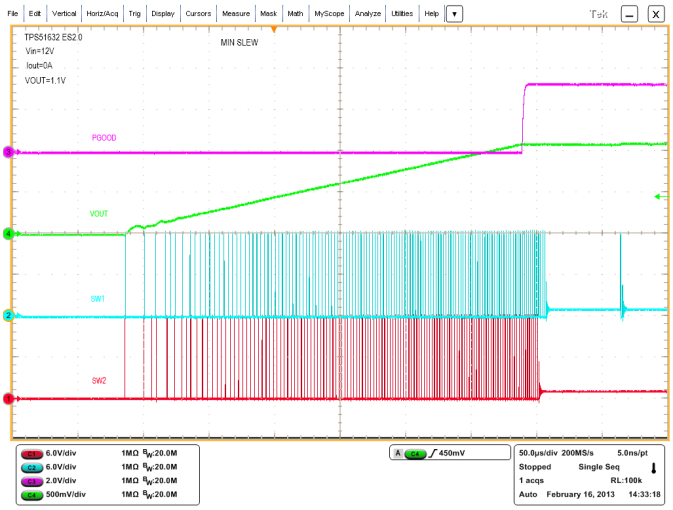


Figure 20. 2-Phase EN Startup

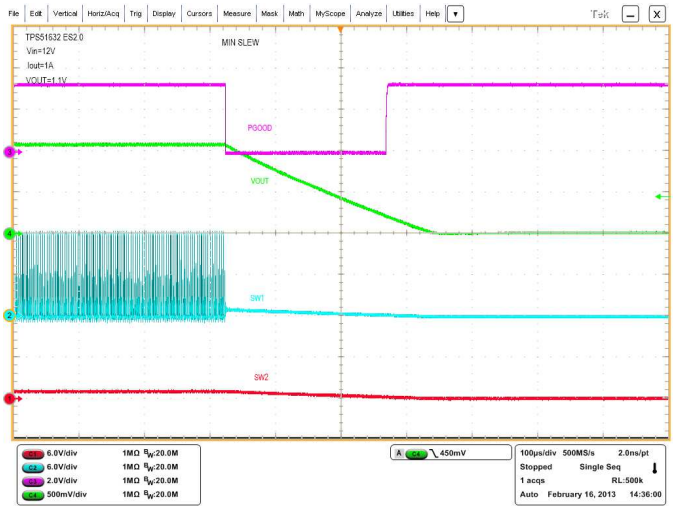


Figure 21. 2-Phase EN Shutdown

TYPICAL CHARACTERISTICS (Output Voltage Transitions)

V_{IN} = 12 V, I_{OUT} = 0 A, Slew Rate: 6 mV/µs

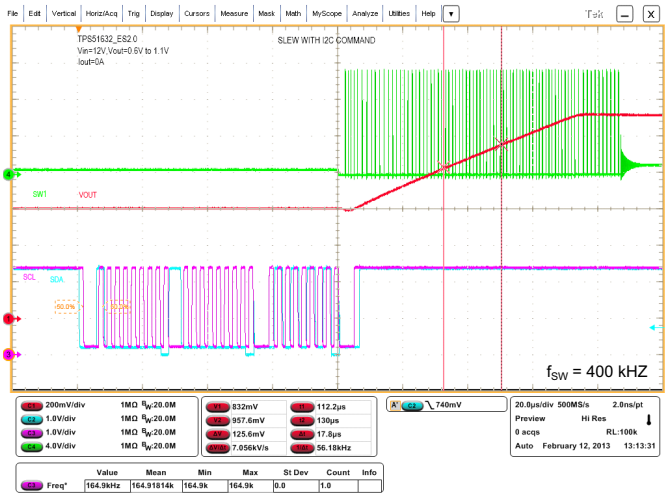


Figure 22. Startup at 400-kHz I²C Clock Speed

Figure 23. Shutdown 400-kHz I²C Clock Speed

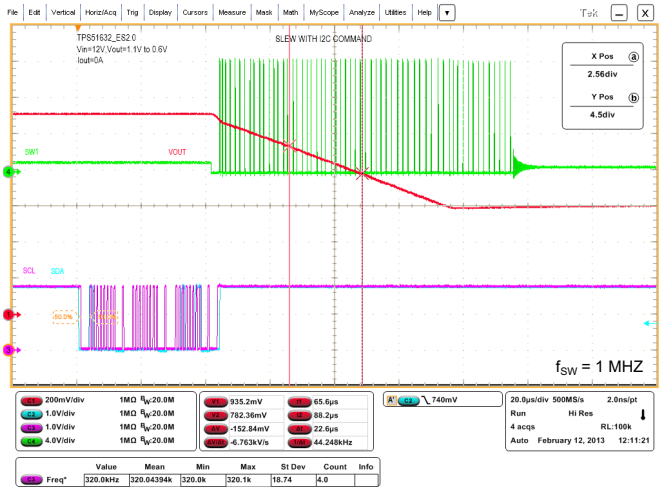


Figure 24. Startup at 1-MHz I²C Clock Speed

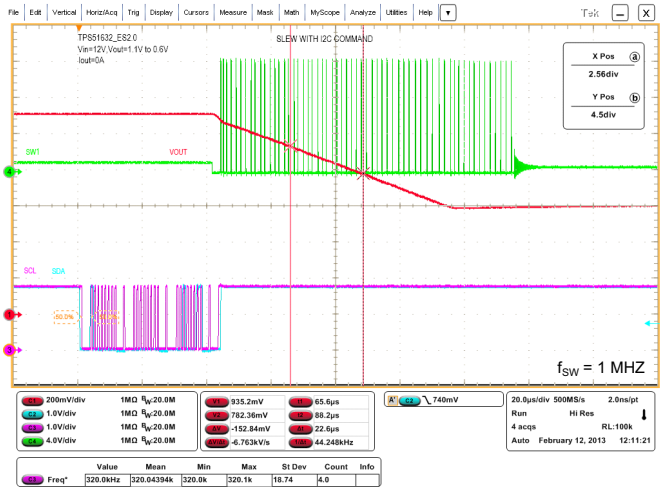


Figure 25. Shutdown 1-MHz I²C Clock Speed

TYPICAL CHARACTERISTICS (Output Voltage Transitions)

V_{IN} = 12 V, I_{OUT} = 10 A, Slew Rate: 6 mV/µs

Figure 26. Startup at 400-kHz I²C Clock Speed

Figure 27. Shutdown 400-kHz I²C Clock Speed

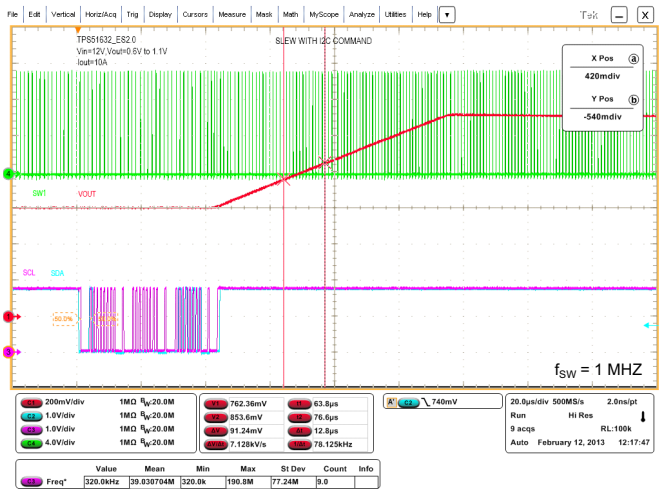


Figure 28. Startup at 1-MHz I²C Clock Speed

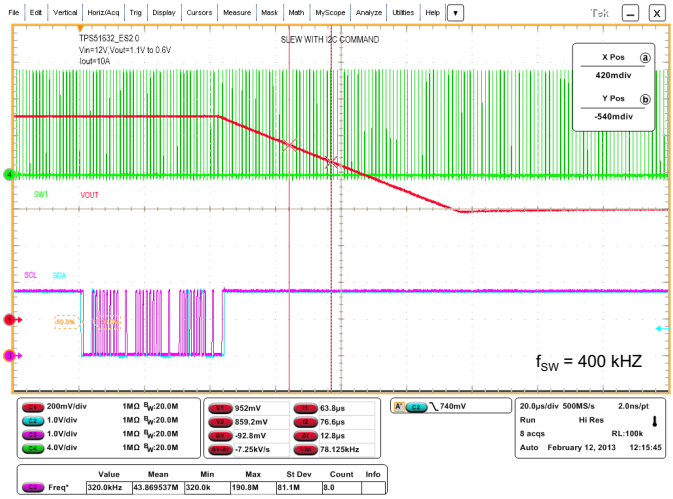


Figure 29. Shutdown 1-MHz I²C Clock Speed

DETAILED DESCRIPTION

Functional Overview

The TPS51632 is a DCAP+ mode adaptive on-time controller. The DAC outputs a reference in accordance with the 8-bit VID code is defined in Table 3. This DAC sets the output voltage.

In adaptive on-time converters, the controller varies the on-time as a function of input and output voltage to maintain a nearly constant frequency during steady-state conditions. With conventional voltage-mode constant on-time converters, each cycle begins when the output voltage crosses to a fixed reference level. However, in the TPS51632, the cycle begins when the current feedback reaches an error voltage level which corresponds to the amplified difference between the DAC voltage and the feedback output voltage. In the case of two-phase or three-phase operation, the device sums the current feedback from all the phases at the output of the internal current-sense amplifiers.

This approach has two advantages:

- The amplifier DC gain sets an accurate linear load-line slope, which is required for CPU core applications.
- The device filters the error voltage input to the PWM comparator to improve the noise performance.

In addition, the difference between the DAC-to-output voltage and the current feedback goes through an integrator to give an approximately linear load-line slope even at light loads where the inductor current is in discontinuous conduction mode (DCM).

During a steady-state condition, the phases of the TPS51631 switch 180° phase-displacement for two-phase mode and 120° phase-displacement for three-phase mode. The phase displacement is maintained both by the architecture (which does not allow the high-side gate drive outputs of more than one phase to be ON in any condition except transients) and the current ripple (which forces the pulses to be spaced equally). The controller forces current-sharing adjusting the ON time of each phase. Current balancing requires no user intervention, compensation, or extra components.

User Selections

After the 5-V, 3.3-V or 1.8-V power is applied to the controller (all are above UVLO level), the following information is latched and cannot be changed anytime during operation. The ELECTRICAL CHARACTERISTICS defines the values of the selections.

- **Operating Frequency.** The resistor from F-IMAX pin to GND sets the switching frequency. See the ELECTRICAL CHARACTERISTICS for the resistor settings corresponding to each frequency selection. It is to be noted that the operating frequency is a quasi-fixed frequency in the sense that the ON time is fixed based on the input voltage (at the VBAT pin) and output voltage (set by VID). The OFF time varies based on various factors such as load and power-stage components.
- **Overcurrent Protection (OCP) Level.** The resistor from OCP-I to GND sets the OCP level of the CPU channel. See the ELECTRICAL CHARACTERISTICS for the resistor settings corresponding to each OCP level.
- **IMON Gain.** The resistors from IMON to OCP-I and OCP-I to GND set the DC load current monitor (IMON) gain.
- **Slew Rate.** The SetVID fast slew rate is set by the resistor from SLEWA pin to GND. See the ELECTRICAL CHARACTERISTICS for the resistor settings corresponding to each slew rate setting.
- **Base Address.** The voltage on SLEWA pin sets the device base address.
- **Ramp Selection.** The resistor from B-RAMP to GND sets the ramp compensation level. See the ELECTRICAL CHARACTERISTICS for the resistor settings corresponding to each ramp level.
- **Boot Voltage.** The output starts-up to the BOOT pin voltage equal to twice the voltage on the B-RAMP pin.
- **Active Phases.** Normally, the controller is configured to operate in 3-phase mode. To enable 2-phase mode, tie the CSP3 pin to a 3.3-V supply and the CSN3 pin to GND. To enable 1-phase mode, tie the CSP2 and CSP3 pins to a 3.3-V supply and tie the CSN2 and CSN3 pins to GND.

PWM Operation

The functional block diagram and Figure 30 show how the converter operates in continuous conduction mode.

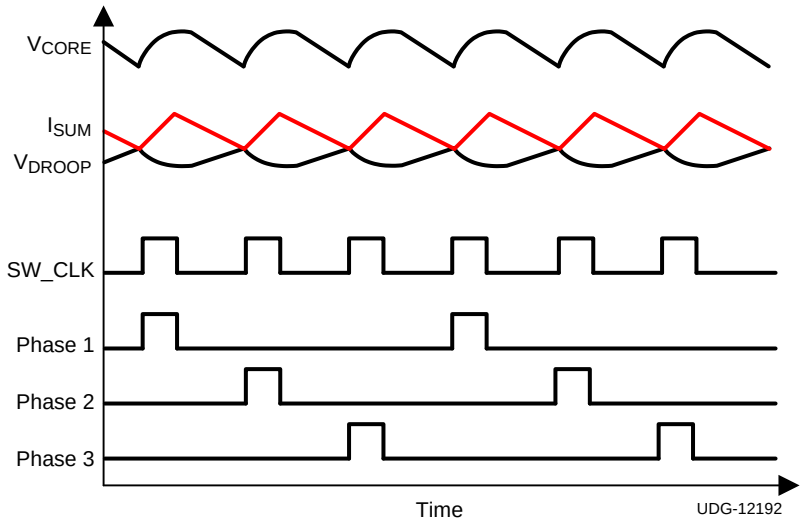


Figure 30. D-CAP+™ Mode Basic Waveforms

Starting with the condition that the high-side FETs are off and the low-side FETs are on, the summed current feedback (I_{SUM}) is higher than the error amplifier output (V_{COMP}). I_{CMP} falls until it hits V_{COMP}, which contains a component of the output ripple voltage. The PWM comparator senses where the two waveforms cross and triggers the on-time generator, which generates the internal SW_CLK signal. Each SW_CLK signal corresponds to one switching ON pulse for one phase.

During single-phase operation, every SW_CLK signal generates a switching pulse on the same phase. Also, I_{SUM} voltage corresponds to a single-phase inductor current only.

During multi-phase operation, the controller distributes the SW_CLK signal to each of the phases in a cycle. Using the summed inductor current and cyclically distributing the ON pulses to each phase automatically gives the required interleaving of 360/n, where n is the number of phases.

Current Sensing

The TPS51632 provides independent channels of current feedback for every phase to increase the system accuracy and reduce the dependence of circuit performance on layout compared to an externally summed architecture. The design can use *inductor DCR sensing* to yield the best efficiency or *resistor current sensing* to yield the most accuracy across wide temperature ranges. DCR sensing can be optimized by using a NTC thermistor to reduce the variation of current sense with temperature.

The pins CSP1, CSN1, CSP2, CSN2 and CSP3, CSN3 are the current sensing pins.

Load Transients

When the load increases suddenly, the output voltage immediately drops. This voltage drop is reflected as a rising voltage on the DROOP pin. This rising voltage forces the PWM to pulse sooner and more frequently which causes the inductor current to rapidly increase. As the inductor current reaches the new load current, a steady-state operating condition is reached and the PWM switching resumes the steady-state frequency. Similarly, when the load releases suddenly, the output voltage rises. This rise is reflected as a falling voltage on the COMP pin. This rising voltage forces a delay in the PWM pulses until the inductor current reaches the new load current, when the switching resumes and steady-state switching continues.

AutoBalance™ Current Sharing

The basic mechanism for current sharing is to sense the average phase current, then adjust the pulse width of each phase to equalize the current in each phase.

The PWM comparator (not shown) starts a pulse when the feedback voltage equals the reference voltage. The VBAT voltage charges $C_{t(on)}$ through the resistor $R_{t(on)}$. The pulse is terminated when the voltage at capacitor $C_{t(on)}$ matches the on-time (t_{ON}) reference, normally the DAC voltage (V_{DAC}).

A current sharing circuit is shown in Figure 31. For example, assume that the 5 µs averaged value of I1 = I2 = I3. In this case, the PWM modulator terminates at V_{DAC}, and the normal pulse width is delivered to the system. If instead, I1 > I_{AVG}, then an offset is subtracted from V_{DAC}, and the pulse width for Phase 1 is shortened, reducing the current in Phase 1 to compensate. If I1 < I_{AVG}, then a longer pulse is produced, again compensating on a pulse-by-pulse basis.

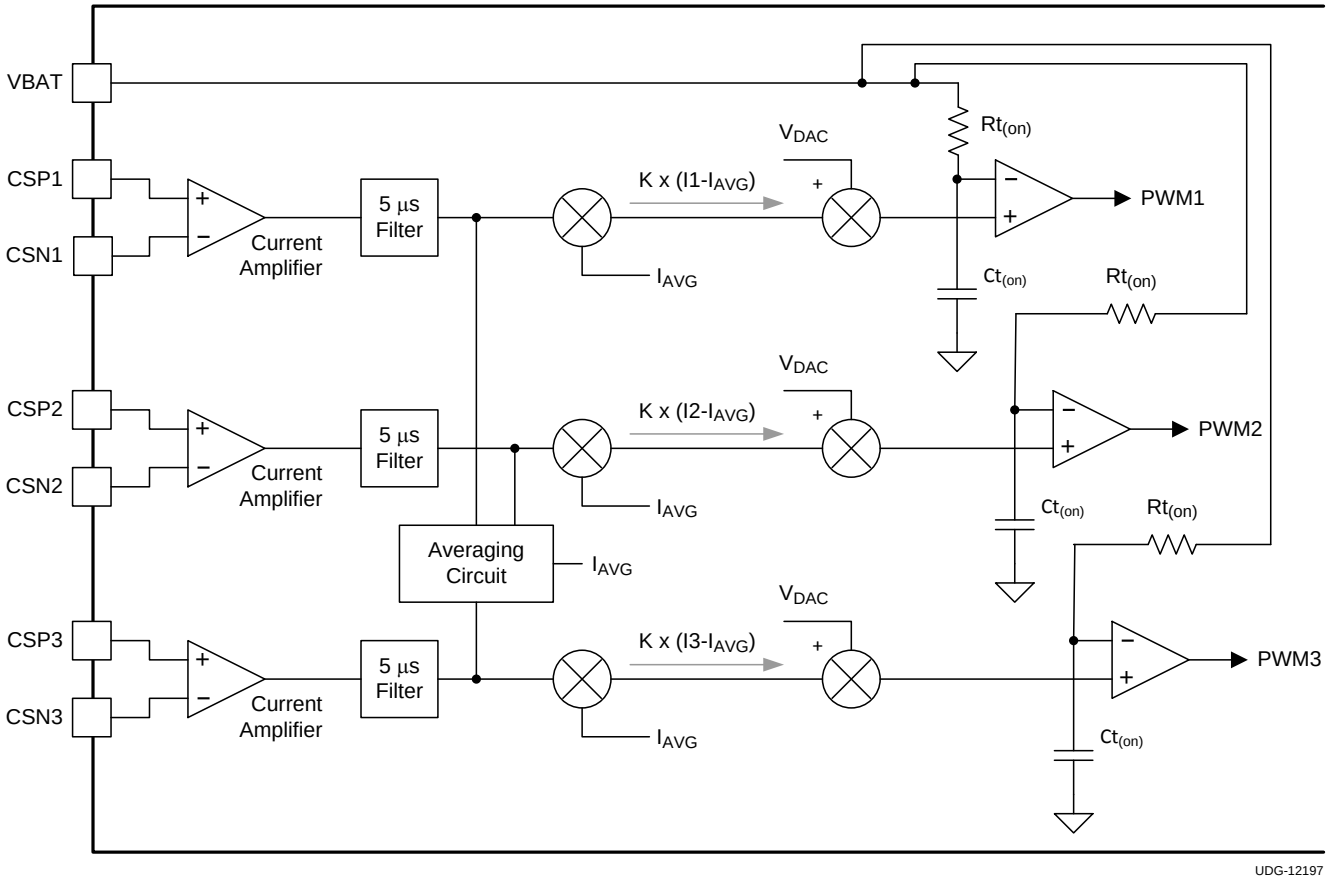


Figure 31. AutoBalance Current Sharing

PWM and $\overline{\text{SKIP}}$ Signals

The PWM and $\overline{\text{SKIP}}$ signals are outputs of the controller and serve as input to the driver or DrMOS type devices. Both are 5-V logic signals. The PWM signals are logic high when the high-side driver turns ON. The PWM signal must be low for the low-side drive to turn ON. When both the drive signals are OFF, the PWM is in tri-state.

5-V, 3.3-V and 1.8-V Undervoltage Lockout (UVLO)

The TPS51632 continuously monitors the voltage on the V5A, VDD and V1P8 pin to ensure a value high enough to bias the device properly and provide sufficient gate drive potential to maintain high efficiency. The converter starts with approximately 4.4 V and has a nominal 200 mV of hysteresis. Once the 5VA or VDD or V18P goes below the V_{UVLOL} , the corresponding voltage must fall below V_{POR} (1.5 V) to reset the device.

The input (V_{BAT}) does not include a UVLO function, so the circuit runs with power inputs as low as approximately 3 x V_{OUT}.

Output Undervoltage Protection (UVP)

Output undervoltage protection works in conjunction with the current protection described in the Overcurrent Protection (OCP) section. If V_{OUT} drops below the low PGOOD voltage threshold, then the drivers are turned OFF until the EN pin power is cycled.

Overcurrent Protection (OCP)

The TPS51632 uses a valley current limiting scheme, so the ripple current must be considered. The DC current value at OCP is the OCP limit value plus half of the ripple current. Current limiting occurs on a phase-by-phase and pulse-by-pulse basis. If the voltage between the CSPx and CSNx pins is above the OCP value, the converter delays the next ON pulse until that voltage difference drops below the OCP limit. For inductor current sensing circuits, the voltage between the CSPx and CSNx pins is the inductor DCR value multiplied by the resistor divider which is part of the NTC compensation network. As a result, a wide range of OCP values can be obtained by changing the resistor divider value. In general, use the highest OCP setting possible with the least attenuation in the resistor divider to provide as much signal to the device as possible. This provides the best performance for all parameters related to current feedback.

In OCP mode, the voltage drops until the UVP limit is reached. Then the converter sets the PGOOD to inactive, and the drivers are turned OFF. The converter remains in this state until the device is reset by the V5A, VDD or V1P8 rails.

Overvoltage Protection

An OVP condition is detected when the output voltage is greater than the PGDH voltage, and greater than VDAC. V_{OUT} > + V_{PGDH} greater than VDAC. In this case, the converter sets PGOOD inactive, and turns ON the drive for the low-side FET. The converter remains in this state until the device is reset by cycling V5A, VDD and V1P8. However, the 350-mV OVP threshold is *blanked* much of the time. In order to provide protection to the processor 100% of the time, there is a second OVP level fixed at V_{OVPH} (approximately 2.5 V) which is always active. If the fixed OVP condition is detected, the PGOOD are forced inactive and the low-side FETs are tuned ON. The converter remains in this state until V5A, VDD or V1P8 is reset.

Analog Current Monitor, IMON and Corresponding Digital Output Current

The TPS51632 includes a current monitor function. The current monitor supplies an analog voltage, proportional to the load current, on the IMON pin.

The current monitor function is related to the OCP selection resistors. The R_{OCP} is the resistor between the OCP-I pin and GND and R_{CIMON} is the resistor between the IMON pin to the OCP-I pin that sets the current monitor gain. Equation 1 shows the calculation for the current monitor gain.

$$V_{IMON} = 10 \times 1 + \frac{(R_{IMON})}{(R_{OCP})} \times \sum V_{CSn} \xrightarrow{yields} V \quad (1)$$

where

- ΣV_{CS} is the sum of the DC voltages at the inputs to the current sense amplifiers

To ensure stable current monitor operation and at the same time provide a fast dynamic response, connect a 4.7-nF capacitor from the IMON pin to GND.

The analog current monitor should be set so that at the maximum processor current ($I_{CC(max)}$) the IMON voltage should be 1.7 V. This corresponds to a digital output current value of 'FF' in register 03H.

Addressing

The TPS51632 can be configured for three different base addresses by setting a voltage on the SLEWA pin. Configure a resistor divider on SLEWA from VREF to GND. As described in the Dynamic Voltage and Frequency Selection (DVFS) section, the resistor from the SLEWA pin to GND sets the slew rate. Once the slew rate resistor is selected, the resistor from the VREF pin to the SLEWA pin can be chosen based on the required base address. For a base address of 0, the VREF to SLEWA resistor can be left open.

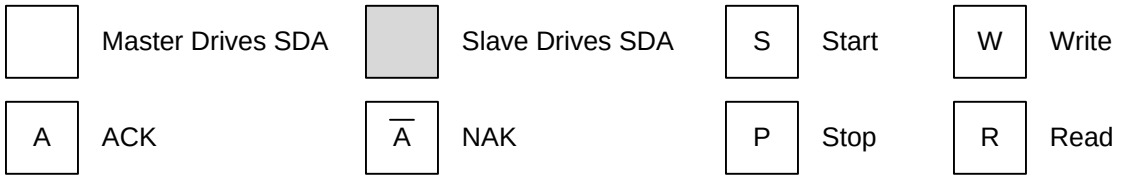
APPLICATION INFORMATION

I²C Interface Operation

TPS51632 includes a slave I²C interface accessed via the SCL (serial clock) and SDA (serial data) pins. The interface sets the base VID value, receives IMON telemetry, and controls functions described in this section. It operates with EN = low, with the bias supplies in regulation. It is compliant with I²C specification UM10204, Revision 3.0; characteristics are detailed below:

- Addressing
  - 7-bit addressing; address range is 100 0xxx (binary)
  - Last three bits are determined by the SLEWA pin at start-up
- Byte read / byte write protocols only (See figures below)
- Frequency
  - 100 kHz
  - 400 kHz
  - 1 MHz
  - 3.4 MHz
- Logic inputs are 1.8 V logic levels (3.3 V tolerant)

Key for Protocol Examples



Protocol Examples

The good byte read transaction the controller ACKs and the master terminates with a NAK/stop

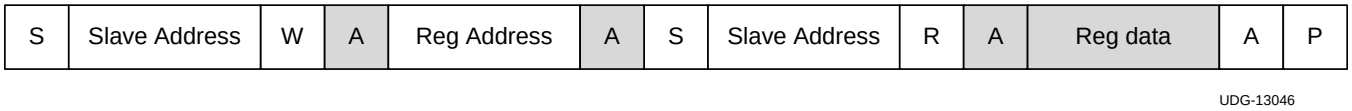


Figure 32. Good Byte Read Transaction

The controller NAKs a read with an invalid register address.

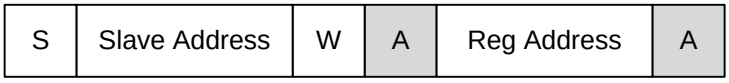


Figure 33. NAK Invalid Register Address

A good byte write is illustrated in Figure 34.

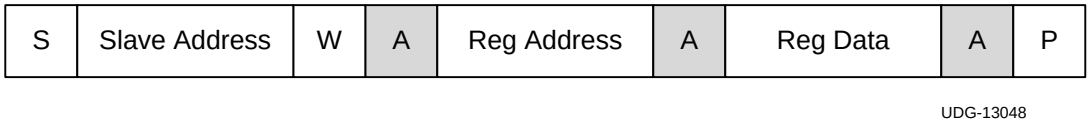


Figure 34. Good Byte Write

The controller NAKs a write with an invalid register address.

Figure 35. Invalid NAK Register Address

The controller will NAK a write for the condition of invalid data.

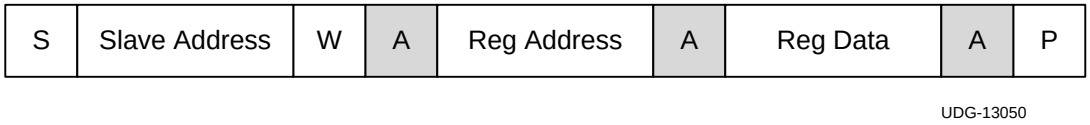


Figure 36. Invalid NAK Register Data

The following master code sequence is executed to enter Hs (3.4 MHz SCL) mode.

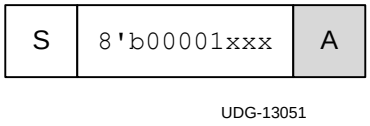


Figure 37. Master Code Sequence

Dynamic Voltage and Frequency Selection (DVFS)

TPS51632 supports DVFS. The converter output voltage is determined by a DAC that receives the sum of two values: the first is the base value; the second is an offset value. The base value shall be 0.5 V or greater. When the VID code is set to 0 V, the DAC slews to 0 V, regardless of the offset value.

DVFS is a digital interface that dynamically changes the DAC offset using the PWM_CLK and PWM_DAT pins as defined below. The function is set up via the following sequence:

1. EN goes high.
2. The base voltage value is set via I^2C.
3. The VMAX register is set via I^2C.
4. Bits are set in register TBD to:
   (a) Set DVFS Step value (10 mV/20 mV).
   (b) Set PGOOD behavior for VMAX (see below).
   (c) Select whether toggling enable will clear the DVFS offset value or retain it.
   (d) Enable DVFS.

The device ignores signals on the PWM_CLK and PWM_DAT pins until DVFS is enabled. DVFS is inactive with EN = LO. The DVFS protocol signals are shown in the figure below:

Refer to NVIDIA document DA-06142-001_V02 for further details.

PWM_CLK signal characteristics are shown in Table 1.

Table 1. DVFS Interface Timing

PARAMETER		CONDITION	MIN	TYP	MAX	UNIT
t_{PWM}	PWM_CLK period		29		300	ns
t_H	PWM high time	PWM_CLK	12		180	
t_L	PWM low time	PWM_CLK	12		180	
t_{DCYC}	PWM duty cycle	PWM_CLK	40%		60%	
t_{SU}	Set-up time	PWM_DAT to rising edge of PWM_CLK	10			ns
t_{HOLD}	Hold time	PWM_DAT from rising edge of PWM_CLK	2			
t_{RISE}	Rise time	PWM_DAT, PWM_CLK	1			
t_{FALL}	Fall time	PWM_DAT, PWM_CLK	1			

The offset operation is shown in Figure 38.

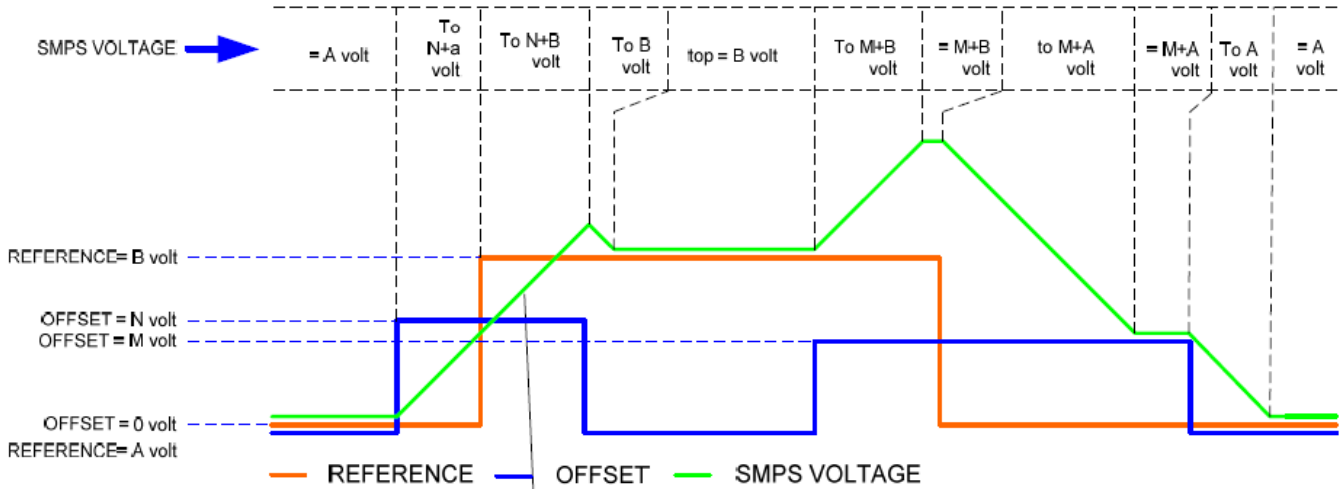


Figure 38. DVFS Reference and Offset Operation

The slew rate for all DVFS transitions is controlled by SLEW pin setting.

NOTE

Both the offset and the reference can change while the voltage is slewing from a prior command.

The VMAX register (address 04h) is set at the factory to 1.28 V. While EN is high, the value may be changed once via I^2C. This value is locked until EN goes low. When EN goes high again, the factory default is restored and the register is unlocked. If a voltage higher than VMAX is requested by any combination of the reference and offset values, the converter shall go to VMAX and no further. The action of PGOOD in this case is controlled by the VMAX_PG bit in the DVFS Control register. If VMAX_PG is high, then PGOOD shall go low when the invalid value is requested and remain low until a new, valid value is requested. The DVFS Control register (address 05h) holds values that determine the detailed behavior of the DVFS interface.

Overcurrent Warning

TPS51632 pulls down the voltage on the PGOOD in whenever the valley current reaches 70% of the OCP value (or higher). PGOOD resumes normal function when the value falls below 65% of the OCP value. I^2C programming enables this function.

TPS51632 Register Definitions

The I^2C interface shall support 400 kHz, 1 MHz, and 3.4 MHz clock frequencies. The I^2C interface shall be accessible even when EN is low. The following registers are accessible via I^2C.

Voltage Select Register (VSR) (Address = 00h)

- Type: Read and write
- Power-up value: BOOT[6:0]
- EN rising (after power-up): prior programmed value
- See Table 3 for exact values
- The VSR is the VID register used when DVFS is not enabled
- A command to set VSR <19h (minimum VID) generatea an NAK and the VSR remains at the prior value

b7	b6	b5	b4	b3	b2	b1	b0
–	VID6	–	–	–	–	–	VID0

VID Base Register (VBR) (Address = 01h)

- Type: Read and write
- Power-up value: 00h
- EN rising (after power-up): prior programmed value
- See Table 3 for exact values
- The VBR is the base register used in DVFS operation
- A command to set VSR <19h (minimum VID) generates an NAK and the VBR remains at the prior value

b7	b6	b5	b4	b3	b2	b1	b0
–	VID6	–	–	–	–	–	VID0

Offset Register (Address = 02h)

- Type: Read only
- Power-up value: 00h
- EN rising (after power-up):00h
- See VID table for exact values
- The offset register is added to the VBR in DVFS operation

b7	b6	b5	b4	b3	b2	b1	b0
–	–	–	MSB	–	–	–	LSB

IMON Register (Address = 03h)

- Type: Read only
- Power-up value: 00h
- EN rising (after power-up):00h

b7	b6	b5	b4	b3	b2	b1	b0
MSB	–	–	–	–	–	–	LSB

VMAX Register (Address = 04h)

- Type: Read / write (see below)
- Power-up value: 1.28V (OTP value)
- EN rising (after power-up): Last written value

b7	b6	b5	b4	b3	b2	b1	b0
Lock	MSB	–	–	–	–	–	LSB

Bit definitions:

BIT	NAME	DEFINITION
0 - 6	VMAX	Maximum VID setting
7	Lock	Access protection of the VMAX register 0: No protection, R/W access to bits 0-6 1: Access is read only; reset after UVLO event.

DVFS Control Register (Address = 05h)

- Type: Read / write
- Power-up value: 00h
- EN rising (after power-up):00h

b7	b6	b5	b4	b3	b2	b1	b0
–	–	FCCM	OCA_EN	PWMRST	VMAX_PG	DVFS_Stp	PWMEN

Bit definitions:

BIT	NAME	'0' DEFINITION	'1' DEFINITION
0	PWMEN	DVFS Off	DVFS On
1	DVFS_Stp	Step = 10mV	Step = 20 mV
2	VMAX_PG	VMAX alarm (VBR + Offset > VMAX) is disabled	VMAX alarm (VBR + Offset > VMAX) is enabled
3	PWMRST	PWMEN unchanged when EN → low	PWMEN cleared when EN → low
4	OCA_EN	Over-current alarm is disabled	Over-current alarm is enabled
5	FCCM	Converter decides CCM/DCM	Forced CCM in all modes

Power State Register (Address = 06h)

- Type: Read and write
- Power-up value: 00h
- EN rising (after power-up):00h

b7	b6	b5	b4	b3	b2	b1	b0
–	–	–	–	–	–	MSB	LSB

Bit definitions:

VALUE	DEFINITION
0	Multi-phase CCM
1	Single-phase CCM
2	Single-phase DCM

SLEW Register (Address = 07h)

- Type: Read and write (see below)
- Power-up value: Defined by SLEWA pin at power-up
- EN rising (after power-up): Last written value
- Write only a single '1' for the SLEW rate desired

b7	b6	b5	b4	b3	b2	b1	b0
48 mV/µs	42mV/µs	36 mV/µs	30 mV/µs	24 mV/µs	18 mV/µs	12 mV/µs	6 mV/µs

Lot Code Registers (Address = 10-13h)

- Type: 8-bits; read only
- Power-up value: Programmed at factory

Fault Register (Address = 14h)

- Type: 8-bits; read only
- Power-up value: 00h

b7	b6	b5	b4	b3	b2	b1	b0
–	–	–	–	Device thermal shutdown	OVP	UVP	OCP

Start-Up Sequence

TPS51632 initializes when all of the supplies rise above the UVLO thresholds. This function is also know as a *cold boot*. The device then reads all of the various settings (such as BOOT pin voltage and overcurrent protection). This process takes less than 1.2 ms. During this time, the VSR initializes to the BOOT voltage (determined by the B-RAMP setting). The output voltage rises to the VSR level when the EN pin (enable) goes high. Once the BOOT sequence completes, PGOOD is HIGH and the I^2C interface can be used to change the voltage select register (VSR). The current VSR value is held when EN goes low and returns to a high state This function is also know as a *warm boot*). The VSR can be changed when EN is low, however, this is not recommended prior to completion of the cold boot process.

Phase Add and Drop Operation

The phase add and drop operation is enabled by default in the TPS51632. The converter starts up in multi-phase CCM mode and reduces phase count until reaching single phase DCM mode as the load is reduced. This action takes place at a fixed percentage of the OCP level defined in the parameter table above. The controller automatically adds phases when the current exceeds the defined percentage of the OCP value. In addition, any USR event sets the converter in multi-phase CCM mode.

To disable the automatic *phase and drop operation*, connect a resistor between the VREF pin and the FREQ-P pin so that the voltage is above the value specified in the parameter table.

Power Good Operation

PGOOD is an open-drain output pin that is designed to be pulled up with an external resistor to a voltage 3.6 V or less. Normal PGOOD operation (exclusive of OC or MAXVID interrupt action) is shown in Figure 39. On initial power-up PGOOD happens within 6 µs of the DAC reaching its target value. When EN is brought low, PGOOD is also brought low for 250 µs and then is allowed to float. TPS51632 pulls down the PGOOD signal when the EN signal subsequently goes high and returns high again within 6 µs of the end of the DAC ramp. The delay period between EN going high and PGOOD going low in this case is less than 1 µs.

Figure 39 shows the power good operation at initial start up and with falling and rising EN.

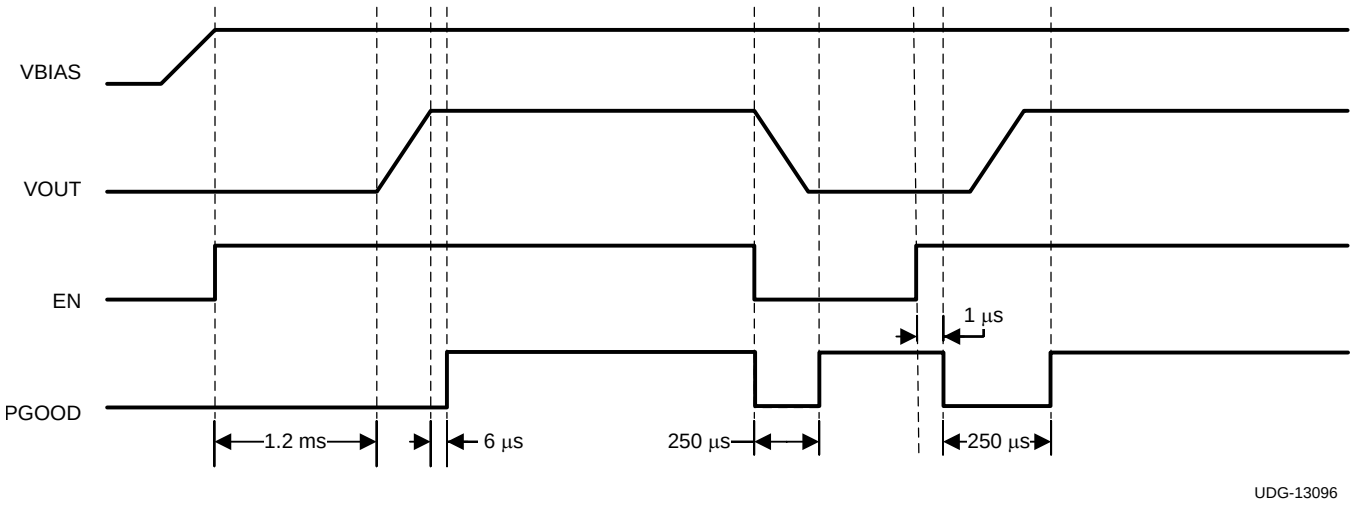


Figure 39. Power Good Operation

Input Voltage Limits

The number of input phases supported varies with the input voltage. See Table 2 for limits. The minimum VIN is lower for lower frequency operation and/or lower output voltages.

Table 2. Input Voltage Limits vs Number of Phases at 1-MHz I²C Clock Speed

NUMBER OF PHASES	$V_{IN(min)}$ (V)	$V_{OUT(max)}$ (V)
3	5.5	1.28
2	3.7	
1	2.5	

Fault Behavior

The TPS51632 has a complete suite of fault detection and protection functions, including input under-voltage lockout on all power inputs, over-voltage and over-current limiting and output under-voltage detection. The protection limits are given in the tables above. The converter suspends switching when the limits are exceeded and PGOOD goes low. In this state, the fault register 14h can be read. To exit fault protection mode, power must be cycled.

Table 3. TPS51632 VID Table

VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	VOLTAGE
0	0	1	1	0	0	1	19	0.5000
0	0	1	1	0	1	0	1A	0.5100
0	0	1	1	0	1	1	1B	0.5200
0	0	1	1	1	0	0	1C	0.5300
0	0	1	1	1	0	1	1D	0.5400
0	0	1	1	1	1	0	1E	0.5500

Table 3. TPS51632 VID Table (continued)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	VOLTAGE
0	0	1	1	1	1	1	1F	0.5600
0	1	0	0	0	0	0	20	0.5700
0	1	0	0	0	0	1	21	0.5800
0	1	0	0	0	1	0	22	0.5900
0	1	0	0	0	1	1	23	0.6000
0	1	0	0	1	0	0	24	0.6100
0	1	0	0	1	0	1	25	0.6200
0	1	0	0	1	1	0	26	0.6300
0	1	0	0	1	1	1	27	0.6400
0	1	0	1	0	0	0	28	0.6500
0	1	0	1	0	0	1	29	0.6600
0	1	0	1	0	1	0	2A	0.6700
0	1	0	1	0	1	1	2B	0.6800
0	1	0	1	1	0	0	2C	0.6900
0	1	0	1	1	0	1	2D	0.7000
0	1	0	1	1	1	0	2E	0.7100
0	1	0	1	1	1	1	2F	0.7200
0	1	1	0	0	0	0	30	0.7300
0	1	1	0	0	0	1	31	0.7400
0	1	1	0	0	1	0	32	0.7500
0	1	1	0	0	1	1	33	0.7600
0	1	1	0	1	0	0	34	0.7700
0	1	1	0	1	0	1	35	0.7800
0	1	1	0	1	1	0	36	0.7900
0	1	1	0	1	1	1	37	0.8000
0	1	1	1	0	0	0	38	0.8100
0	1	1	1	0	0	1	39	0.8200
0	1	1	1	0	1	0	3A	0.8300
0	1	1	1	0	1	1	3B	0.8400
0	1	1	1	1	0	0	3C	0.8500
0	1	1	1	1	0	1	3D	0.8600
0	1	1	1	1	1	0	3E	0.8700
0	1	1	1	1	1	1	3F	0.8800
1	0	0	0	0	0	0	40	0.8900
1	0	0	0	0	0	1	41	0.9000
1	0	0	0	0	1	0	42	0.9100
1	0	0	0	0	1	1	43	0.9200
1	0	0	0	1	0	0	44	0.9300
1	0	0	0	1	0	1	45	0.9400
1	0	0	0	1	1	0	46	0.9500
1	0	0	0	1	1	1	47	0.9600
1	0	0	1	0	0	0	48	0.9700
1	0	0	1	0	0	1	49	0.9800
1	0	0	1	0	1	0	4A	0.9900
1	0	0	1	0	1	1	4B	1.0000
1	0	0	1	1	0	0	4C	1.0100
1	0	0	1	1	0	1	4D	1.0200

Table 3. TPS51632 VID Table (continued)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	VOLTAGE
1	0	0	1	1	1	0	4E	1.0300
1	0	0	1	1	1	1	4F	1.0400
1	0	1	0	0	0	0	50	1.0500
1	0	1	0	0	0	1	51	1.0600
1	0	1	0	0	1	0	52	1.0700
1	0	1	0	0	1	1	53	1.0800
1	0	1	0	1	0	0	54	1.0900
1	0	1	0	1	0	1	55	1.1000
1	0	1	0	1	1	0	56	1.1100
1	0	1	0	1	1	1	57	1.1200
1	0	1	1	0	0	0	58	1.1300
1	0	1	1	0	0	1	59	1.1400
1	0	1	1	0	1	0	5A	1.1500
1	0	1	1	0	1	1	5B	1.1600
1	0	1	1	1	0	0	5C	1.1700
1	0	1	1	1	0	1	5D	1.1800
1	0	1	1	1	1	0	5E	1.1900
1	0	1	1	1	1	1	5F	1.2000
1	1	0	0	0	0	0	60	1.2100
1	1	0	0	0	0	1	61	1.2200
1	1	0	0	0	1	0	62	1.2300
1	1	0	0	0	1	1	63	1.2400
1	1	0	0	1	0	0	64	1.2500
1	1	0	0	1	0	1	65	1.2600
1	1	0	0	1	1	0	66	1.2700
1	1	0	0	1	1	1	67	1.2800
1	1	0	1	0	0	0	68	1.2900
1	1	0	1	0	0	1	69	1.3000
1	1	0	1	0	1	0	6A	1.3100
1	1	0	1	0	1	1	6B	1.3200
1	1	0	1	1	0	0	6C	1.3300
1	1	0	1	1	0	1	6D	1.3400
1	1	0	1	1	1	0	6E	1.3500
1	1	0	1	1	1	1	6F	1.3600
1	1	1	0	0	0	0	70	1.3700
1	1	1	0	0	0	1	71	1.3800
1	1	1	0	0	1	0	72	1.3900
1	1	1	0	0	1	1	73	1.4000
1	1	1	0	1	0	0	74	1.4100
1	1	1	0	1	0	1	75	1.4200
1	1	1	0	1	1	0	76	1.4300
1	1	1	0	1	1	1	77	1.4400
1	1	1	1	0	0	0	78	1.4500
1	1	1	1	0	0	1	79	1.4600
1	1	1	1	0	1	0	7A	1.4700
1	1	1	1	0	1	1	7B	1.4800
1	1	1	1	1	0	0	7C	1.4900

Table 3. TPS51632 VID Table (continued)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	VOLTAGE
1	1	1	1	1	0	1	7D	1.5000
1	1	1	1	1	1	0	7E	1.5100
1	1	1	1	1	1	1	7F	1.5200

DESIGN EXAMPLE

Introduction

The TPS51632 has a very simple design procedure.Microsoft Excel®-based component value calculation tool is available. Please contact your local TI representative to get a copy of the spreadsheet.

Design example specifications:

- Number of phases: 2
- Input voltage range: 7.4 V to 20 V
- V_{PS0} = 1.0 V
- $I_{CC(max)}$ = 21 A
- $I_{DYN(max)}$ = 16 A
- $I_{CC(TDC)}$ = 16 A
- Slew rate (minimum): 24 mV/µs

Step One: Select Switching Frequency

The switching frequency is selected by a resistor from FREQ_P to GND (R_F). The frequency is an approximate frequency and is expected to vary based on load and input voltage.

Table 4. TPS51632 Frequency Selection Table

SELECTION RESISTOR (R_F) VALUE (kΩ)	OPERATING FREQUENCY (f_{SW}) (kHz)
24	400
39	600
75	800
150	1000

For this design, choose a switching frequency of 600 kHz. So, R_F = 39 kΩ.

Step Two: Set the Slew Rate

A resistor to GND (R_{SLEW}) on SLEWA pin sets the slew rate. For a minimum 24 mV/µs slew rate, the resistor R_{SLEW} = 39 kΩ.

Table 5. Slew Rate vs. Selection Resistor

SELECTION RESISTOR R_{SLEW} (kΩ)	MINIMUM SLEW RATE (mV/µs)
39	24
56	30
75	36
100	42
150	48

NOTE

The voltage on the SLEWA pin also sets the base address. For a base address of 00, the SLEWA pin should have only one resistor, R_{SLEW} to GND. For other base addresses, a resistor can be connected between the SLEWA pin and the VREF pin (1.7 V). This resistor can be calculated to set the corresponding voltage for the required address listed in Table 6.

Table 6. Address Selection

SLEWA VOLTAGE	BASE ADDRESS
V_{SLEWA} ≤ 0.30 V	0
0.75 V ≤ V_{SLEWA} ≤ 0.85 V	3
1.15 V ≤ V_{SLEWA} ≤ 1.25 V	5

Step Three: Determine Inductor Value and Choose Inductor

Applications with smaller inductor values have better transient performance but also have higher voltage ripple and lower efficiency. Applications with higher inductor values have the opposite characteristics. It is common practice to limit the ripple current to 20% to 40% of the maximum current per phase. In this case, use 30%.

$$I_{P-P} = \frac{21(A)}{2} \times 0.4 = 4.2\ (A) \tag{2}$$

$$L = \frac{V \times dT}{I_{P-P}} \tag{3}$$

In this equation,

$$V = V_{IN(max)} - V_{OUT} - 19\ V \tag{4}$$

$$\frac{V_{OUT}}{\left(f \times V_{IN(max)}\right)} = 83\ ns \tag{5}$$

$$I_{P-P} = 4.2\ A \tag{6}$$

$$I_{P-P} = \frac{21(A)}{2} \times 0.4 = 4.2\ (A) \tag{7}$$

So, calculating, L=0.376 µH.

Choose an inductance value of 0.33 µH. The inductor must not saturate during peak loading conditions.

$$I_{SAT} = \left(\frac{I_{CC(max)}}{N_{PH}} + \frac{I_{P-P}}{2}\right) \times 1.2 = 15\ A \tag{8}$$

The factor of 1.2 allows for current sensing and current limiting tolerances.

The chosen inductor should have the following characteristics:

- as flat as an inductance vs. current curve as possible. Inductor DCR sensing is based on the idea L/DCR is approximately a constant through the current range of interest
- either high saturation or *soft saturation*
- low DCR for improved efficiency, but at least 0.6 mΩ for proper signal levels
- DCR tolerance as low as possible for load-line accuracy

For this application, choose a 0.33-µH, 6.8-mΩ inductor.

Step Four: Determine Current Sensing Method

The TPS51632 supports both resistor sensing and inductor DCR sensing. Inductor DCR sensing is chosen. For resistor sensing, substitute the resistor value (between approximately 3 mΩ and 4 mΩ) recommended for a 2-phase 21-A application) for $R_{CS(eff)}$ in the subsequent equations.

Step Five: DCR Current Sensing

Design the thermal compensation network and selection of OCP. In most designs, NTC thermistors are used to compensate thermal variations in the resistance of the inductor winding. This winding is generally copper, and so has a resistance coefficient of 3900 PPM/°C. NTC thermistors, as an alternative, have very non-linear characteristics and need two or three resistors to linearize them over the range of interest. A typical DCR circuit is shown in Figure 40.

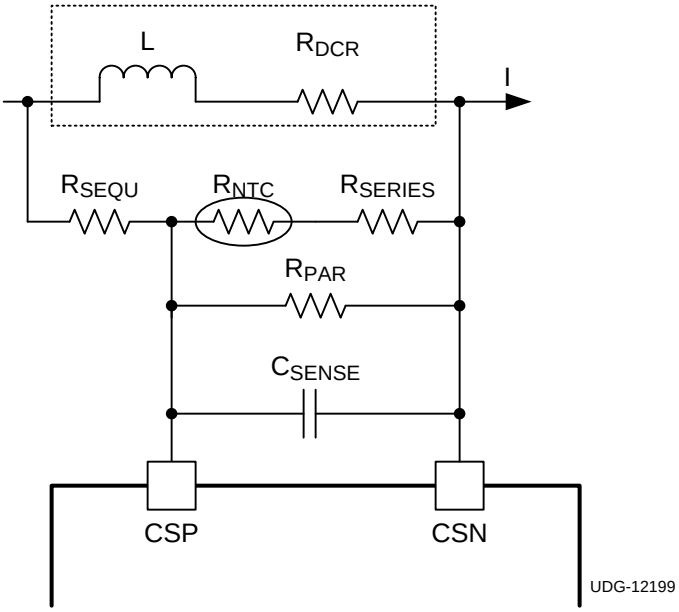


Figure 40. Typical DCR Sensing Circuit

In this design example, the voltage across the C_{SENSE} capacitor exactly equals the voltage across R_{DCR} when:

$$\frac{L}{R_{DCR}} = C_{SENSE} \times R_{EQ} \tag{9}$$

$$R_{EQ} = \frac{R_{P\_N}}{R_{SEQU} - R_{P\_N}}$$

where

- R_{EQ} is the series (or parallel) combination of R_{SEQU}, R_{NTC}, R_{SERIES} and R_{PAR} (10)

$$R_{P\_N} = \frac{R_{PAR} \times (R_{NTC} + R_{SERIES})}{R_{PAR} + R_{NTC} + R_{SERIES}} \tag{11}$$

Ensure that C_{SENSE} is a capacitor type which is stable over temperature. Use X7R or better dielectric (C0G preferred).

Because calculating these values by hand is difficult, TI offers a spreadsheet using the Excel *Solver* function available to calculate them for you. Please contact your local TI representative to get a copy of the spreadsheet.

In this design, the following values are input to the spreadsheet.

- L = 0.33 µH
- R_{DCR} = 6.8 mΩ
- Minimum Overcurrent Limit = 30 A
- Thermistor R25 = 10 kΩ and “B” value = 3380 kΩ

The spreadsheet then calculates the OCP (overcurrent protection) setting and the values of R_{SEQU}, R_{SERIES}, R_{PAR}, and C_{SENSE}. In this case, the OCP setting is the resistor value selection of 100 kΩ from OCP-I to GND. The nearest standard component values are:

- R_{SEQU} = 3.39 kΩ
- R_{SERIES} = 2.96 kΩ
- R_{PAR} = 5.18 kΩ
- C_{SENSE} = 27 nF

Consider the effective divider ratio for the inductor DCR. The effective current sense resistance ($R_{CS(eff)}$ is shown in Equation 12.

$$R_{CS(eff)} = R_{DCR} \times \frac{R_{P\_N}}{R_{SEQU} + R_{P\_N}} \quad (12)$$

R_{P_N} is the series/parallel combination of R_{NTC}, R_{SERIES} and R_{PAR}.

$$R_{P\_N} = \frac{R_{PAR} \times (R_{NTC} + R_{SERIES})}{R_{PAR} + R_{NTC} + R_{SERIES}} \quad (13)$$

$R_{CS(eff)}$ is 3.5 mΩ.

Step Six: Select OCP Level

Set the OCP threshold level that corresponds to Equation 14.

$$I_{VALLEY} \times R_{CS(eff)} = V_{CS(ocp)} \quad (14)$$

$$I_{VALLEY} = \frac{I_{OCP}}{N_{PH}} - 0.5 - I_{RIPPLE} \quad (15)$$

Table 7. OCP Selection(1)

SELECTION RESISTOR R_{OCP} (kΩ)	TYPICAL $V_{CS(OCP)}$ (mV)
3	19
56	25
75	32
100	40
150	49

(1) If a corresponding match is not found, then select the next higher setting.

Step Seven: Determine the Output Capacitor Configuration

The amount of output capacitance needed for this design is function of both loop stability and transient requirement.

Transient Consideration

Design specifications:

- $I_{DYN(max)}$ = 16 A
- di/dt > 100 A/µs
- V_{OUT} deviation = ±3% for the above given transient

Use the following Equation 16 and Equation 17 to estimate the amount of capacitance needed for a given dynamic load or release.

$$C_{OUT(\text{min\_under})} = \frac{\mathrm{L} \times \Delta I_{LOAD(max)}{}^2 \times \left(\frac{V_{OUT} \times t_{SW}}{V_{IN(min)}} + t_{MIN(off)}\right)}{2 \times \Delta I_{LOAD(insert)} \times \left(\left(\frac{V_{IN(min)} - V_{OUT}}{V_{IN(min)}}\right) \times t_{SW} - t_{MIN(off)}\right) \times V_{OUT}} \quad (16)$$

$$C_{OUT(\text{min\_over})} = \frac{\mathrm{L} \times \Delta I_{LOAD(max)}{}^2}{2 \times \Delta I_{LOAD(release)} \times V_{OUT}}$$

where

- L = ½ x L_{OUT} per phase
- $t_{MIN(off)}$ = 80 ns (17)

Based on the calculation, to meet the transient requirement, the minimum amount of capacitance is 704 µF. Use 2 (two) 330-µF (6 mΩ) and 2 (two) 22-µF as the output capacitors.

Stability Consideration

The TPS51632 control architecture (current mode, constant on-time) has been analyzed by the Center for Power Electronics Systems (CPES) at Virginia Polytechnic and State University. The following equations are from the presentation: *Equivalent Circuit Representation of Current-Mode Control* from November 21, 2008.

A simplified control loop diagram is shown in Figure 41. One of the benefits of this technology is the lack of the sample and hold effect that limits the bandwidth of fixed frequency current mode controllers and causes sub-harmonic oscillations.

The open loop gain, G_{OL}, is the gain of the error amplifier, multiplied by the control-to-output gain and is calculated in Equation 18.

$$G_{OL} = G_{COMP} \times G_{CO} \tag{18}$$

The control-to-output gain circuitry is shown in Figure 41.

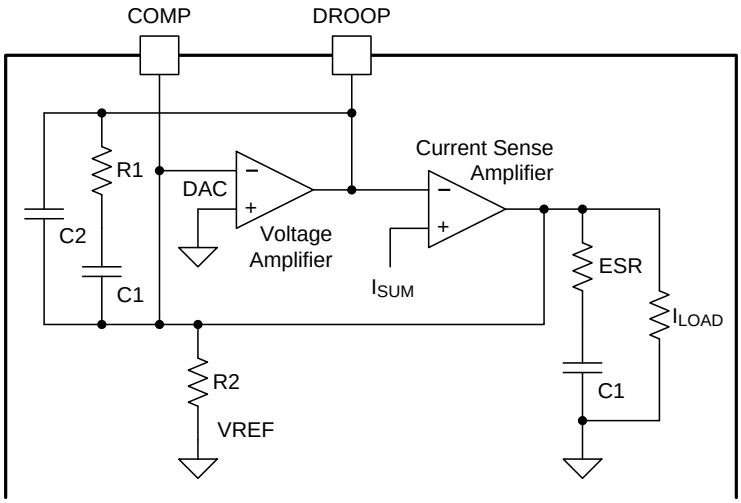


Figure 41. Control to Output Gain Circuitry

The control-to-output gain is calculated in Equation 19.

$$\frac{v_O}{v_C} = K_C \times \frac{1}{1 + \left(\frac{\omega}{Q_1 \times \omega_1}\right) + \left(\frac{\omega^2}{{\omega_1}^2}\right)} \times \frac{(\omega \times R_{ESR} \times C_{OUT}) + 1}{\left(\frac{\omega}{\omega_a}\right) + 1}$$

where

- $K_C = \dfrac{\left(\frac{R_{LOAD}}{R_i}\right)}{1 + \left(\frac{t_{ON} \times R_{LOAD}}{2 \times L_S}\right)}$
- $\omega_1 = \dfrac{\pi}{t_{ON}}$
- $Q_1 = \dfrac{2}{\pi}$
- $t_{ON} = \dfrac{V_{OUT}}{V_{IN} \times f_{SW}}$

- $$\omega_a = \frac{1 + \left(\frac{t_{ON} \times R_{LOAD}}{2 \times L_S}\right)}{R_{LOAD} \times C_{OUT} \times \left(1 + \left(\frac{t_{ON} \times R_{LOAD}}{2 \times L_S}\right)\right)} \quad (19)$$

For this converter, $R_i = R_{CS(eff)} \times A_{CS}$

The theoretical control-to-output transfer function shows 0-dB bandwidth is approximately 20 kHz and the phase margin is greater than 90°. As a result, creating the desired loop response is a matter a adding an appropriate pole-zero or pole-zero-pole compensation for the high-gain system.

The loop compensation is designed to meet the following criteria:

1. Phase margin ≥ 60°
   (a) Not only is more stable, but settles more quickly for repetitive transients
2. Bandwidth: $\frac{f_{SW}}{5} \geq BW \geq \frac{f_{SW}}{3}$
   (a) High enough BW for good transient response.
   (b) If too high, the response for the voltage changes gets very “bumpy”, as each voltage step causes several pulses very quickly.
3. The phase angle of the compensation at the switching frequency needs to be very near to 0 degrees (resistive)
   (a) Otherwise, there is a phase shift between DROOP and ISUM
   (b) Practically, this means the zero frequency should be < $f_{SW}/2$, and any high frequency pole (for noise rejection) needs to be > 2 x f_{SW}.

The voltage error amplifier is used in the design. The compensation technique used here is a type II compensator which is shown in **Figure TBD**. Equation 20 describes the transfer function, which has a pole that occurs at the origin. The type II amplifier also has a zero (f_Z) that can be programmed by selecting R1 and C1 values. In addition, the type II compensation network has a pole (f_P) that can be programmed by selecting R1 and C2.

$$G_{COMP} = \frac{1}{s \times (C1 + C2) \times R2} \times \frac{(s \times R1 \times C1 + 1)}{s \times R1 \times \left(\frac{C1 \times C2}{C1 + C2}\right) + 1} \quad (20)$$

$$f_Z = \frac{1}{2\pi \times R1 \times C1} \quad (21)$$

$$f_P = \frac{1}{2\pi \times R1 \times \frac{C1 \times C2}{C1 + C2}} \quad (22)$$

R1 sets the loop crossover to correct for the gain at control to output function. In this design, select R2 = 2 kΩ. To cross over the voltage loop at around 150 kHz requires R1 to equal 6.3 kΩ.

$$R1 = R2 \times 10^{\frac{-Gco(fc)}{20}} = 2k \times 10^{\frac{-(-10dB)}{20}} = 6.3\ k\Omega \quad (23)$$

In this design, a standard 1% resistor of 6.49 kΩ is used. Capacitor C1 adds phase margin at crossover frequency and can be set between 10% and 20% of the switching frequency.

$$C1 = \frac{1}{2\pi \times f_{SW} \times 10\% \times R1} = 408\ pF \quad (24)$$

For this design a standard capacitor value of 470 pF is used. The last consideration to the voltage loop compensation design is C2. The purpose of C2 is to cancel the phase gain caused by the ESR of the output capacitor in the control-to-output function after the loop crossover. To make sure the gain continues to roll off after the voltage loop crossover, the C2 is selected to meet Equation 25.

$$C2 = \frac{C_{OUT} \times ESR}{R1} = 305\ pF \quad (25)$$

For this design, a standard capacitor value of 330 pF is used. Contact your TI representative to obtain a copy of the spreadsheet program used to calculate the stability requirement in this section.

Step Eight: Current Monitor (IMON) setting

The analog current monitor should be set so that at $I_{CC(max)}$ the IMON pin voltage should be 1.7 V. This corresponds to a digital I_{OUT} value of 'FF' in I^2C register 03H. The voltage on the IMON pin is shown in Equation 26.

$$V_{IMON} = 10 \times 1 + \frac{(R_{IMON})}{(R_{OCP})} \times \sum V_{CSn} \xrightarrow{yields} V \tag{26}$$

So,

$$1.7 = 10 \times \left(1 + \frac{R_{IMON}}{R_{OCP}}\right) \times R_{CS(eff)} \times I_{CC(max)} \tag{27}$$

here

- $I_{CC(max)}$= 21 A
- $R_{CS(eff)}$ is 3.5 mΩ
- R_{OCP} is 100 kΩ

Solving, R_{IMON} = 132 kΩ. R_{IMON} is connected from IMON pin to OCP-I pin.

PCB LAYOUT GUIDELINES

Schematic Review

- Check the pin-out of the controller on schematic against the pin-out of datasheet.
- Get a closest TI reference design to check for connections and component values.
- Have a component value calculator tool ready to check component values.
- Carefully check choice of inductor and DCR.
- Carefully check choice of output capacitors.
- Because the voltage and current feedback signals are fully differential it is a good idea to double check their polarity.
  - CSP1 / CSN1
  - CSP2 / CSN2
  - CSP3 / CSN3
  - VOUT_SENSE to VFB / GND_SENSE to GFB
- Make sure the pull-up on the SDA, SCL, PWM_DT and PWM_CL lines are correct. Check if there is a by-pass capacitor close to the device on the pull-up V1P8 rail to GND of the device.
- Strongly recommend that the device GND be separate from the system and Power GND.

NOTE

Make sure to separate noisy driver interface lines. This is a critical layout rule.

The TPS51632 makes this easy. The driver (TPS51604) is outside of the device. All gate-drive and switch-node traces must be local to the inductor and MOSFETs.

Current Sensing Lines

Given the physical layout of most systems, the current feedback (CSPx, CSNx) may have to pass near the power chain. Clean current feedback is required for good load-line, current sharing, and current limiting performance of the TPS51632, so please take the following precautions.

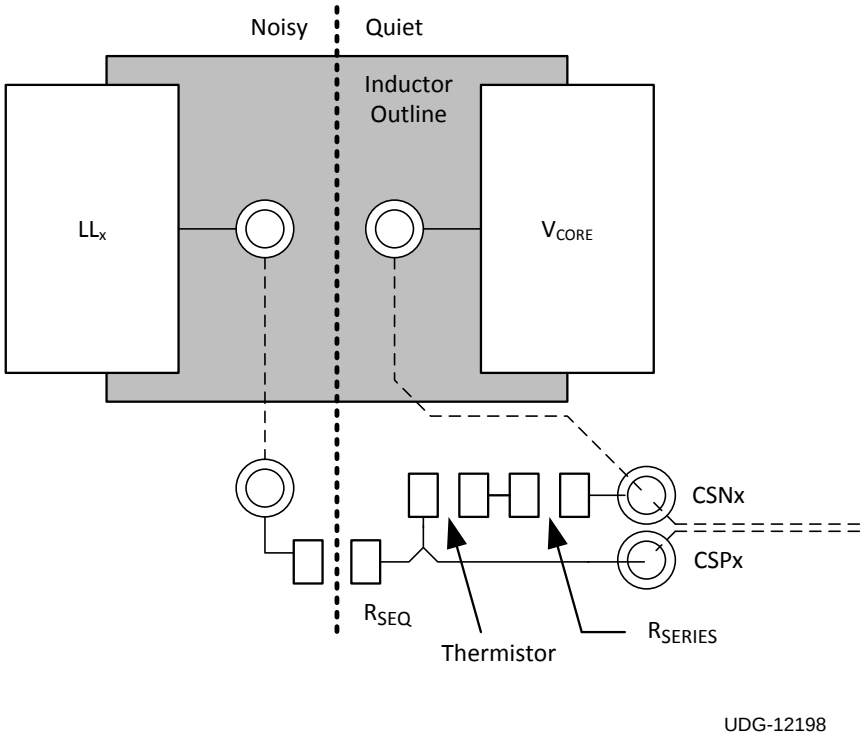


Figure 42. Kelvin Connections to the Inductor for DCR Sensing

- Ensure all vias in the CSPx and CSNx traces are isolated from all other signals.
- Dotted signal traces are recommended to be run in internal planes.
- If possible, change the name of the CSNx trace if possible to prevent automatic ties to the V_{CORE} plane.
- Put R_{SEQU} at the boundary between noisy and quiet areas.
- Run CSPx and CSNx as a differential pair in a quiet layer.
- Place the capacitor as near to the device pins as possible.
- Make a Kelvin connection to the pads of the resistor or inductor used for current sensing. See Figure 42 for a layout example.
- Run the current feedback signals as a differential pair to the device.
- Run the lines in a quiet layer. Isolate the lines from noisy signals by a voltage or ground plane.
- Put the compensation capacitor for DCR sensing (C_{SENSE}) as close to the CS pins as possible.
- Place any noise filtering capacitors directly under or near the TPS51632 and connect to the CS pins with the shortest trace length possible.

Feedback voltage Sensing lines

The voltage feedback coming from the CPU socket must be routed as differential pair all the way to the TPS51632 VFB and GFB pins. Care should be taken to avoid routing over Switch-node and Gate-drive traces.

I²C and DVFS lines

The routing of the I²C and DVFS lines (pin 1, SDA; pin 31, SCL; pin 32, PWM_DT and pin 30, PWM_CL) should be as per NVIDIA recommendation. These traces should follow the impedance matching as specified by NVIDIA. Place a 0.1-µF bypass capacitor from the V1P8 pin (which is the pull-up rail for both I²C and DVFS termination resistors) to GND as close to the device as possible.

PWM and $\overline{\text{SKIP}}$ Lines

The PWM and $\overline{\text{SKIP}}$ lines should be routed from TPS51632 to the driver without crossing any switch-node or the gate drive signals.

Minimize High Current Loops

Figure 43 above shows the primary current loops in each phase, numbered in order of importance.

The most important loop to minimize the area of is Loop 1, the path from the input capacitor through the high and low-side FETs, and back to the capacitor through ground.

Loop 2 is from the inductor through the output capacitor, ground and Q2. The layout of the low-side gate drive (Loops 3a and 3b) is important. The guidelines for gate drive layout are:

- Make the low-side gate drive as short as possible (1 inch or less preferred).
- Make the DRVL width to length ratio of 1:10, wider (1:5) if possible.
- If changing layers is necessary, use at least two vias.

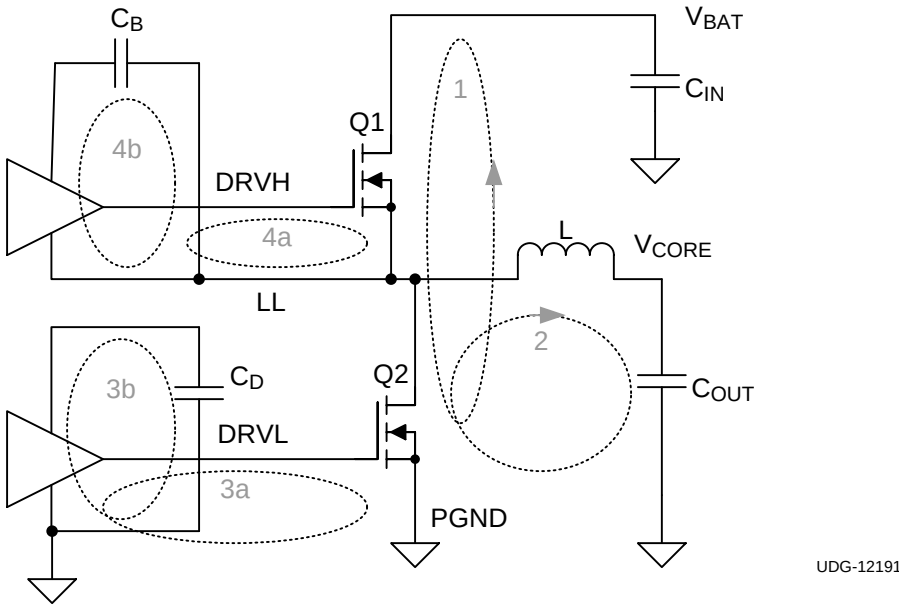


Figure 43. Major Current Loops to Minimize

Power Chain Symmetry

The TPS51632 does not require special care in the layout of the power chain components. This is because independent isolated current feedback is provided. If it is possible to lay out the phases in a symmetrical manner, then please do so. The rule is: the current feedback from each phase needs to be clean of noise and have the same effective current sense resistance.

Component Location

Place components as close to the device in the following order.

1. CS pin noise filtering components,
2. COMP pin and DROOP pin compensation components,
3. Decoupling capacitors for VREF, VDD, V5A, V1P8
4. Decoupling cap for V1P8 rail which is pull-up voltage for the digital lines. This decoupling should be placed near the device to have good signal integrity.
5. OCP-I resistors, FREQ_P resistors, SLEWA resistors, and B-RAMP resistors.

Grounding Recommendations

The TPS51632 has an analog ground and a thermal pad. The normal procedure for connecting these is:

- Keep the analog GND of the device and the power GND of the power circuit separate. The device analog GND and the power circuit power GND can be connected at one single quite point in the layout.
- The thermal pad is not having an electrical connection to device. But this must be connected to Pin 29 GND of the device to give good ground shielding. Do not connect this to system GND.
- Tie the thermal pad to a ground island with at least 4 vias. All the analog components can connect to this analog ground island.
- The analog ground can be connected to any quiet spot on the system ground. A quiet spot is defined as a spot where no power supply switching currents are likely to flow. Use a single point connection from analog ground to the system ground.
- Make sure the bottom FET source connection and the input decoupling capacitors have plenty of vias.

Decoupling Recommendations

- Decouple V5A and VDD to GND with a ceramic capacitor (with a value of at least 1-µF) .
- Decouple V1P8 to GND with a capacitor (with a value of at least 0.1-µF) to GND.

Conductor Widths

- Follow NVIDIA guidelines with respect to the voltage feedback and logic interface connection requirements.
- Maximize the widths of power, ground and drive signal connections.
- For conductors in the power path, be sure there is adequate trace width for the amount of current flowing through the traces.
- Make sure there are sufficient vias for connections between layers. Use 1 minimum via per ampere of current.

REVISION HISTORY

Changes from Original (APRIL 2013) to Revision A **Page**

- Added Typical Characteristics section 11
- Added Application Information section 22
- Added Design Example 33

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS51632RSMR	ACTIVE	VQFN	RSM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-10 to 105	TPS 51632	Samples
TPS51632RSMT	ACTIVE	VQFN	RSM	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-10 to 105	TPS 51632	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

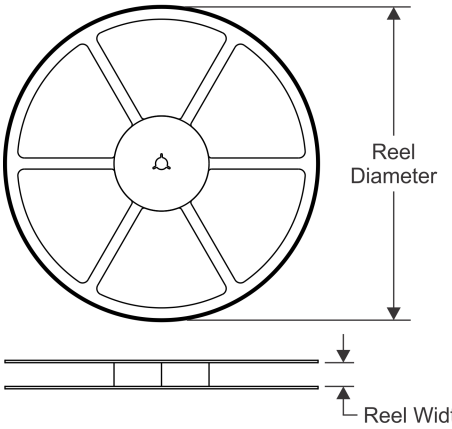
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

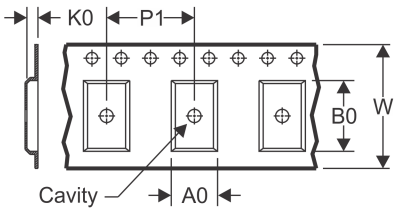
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

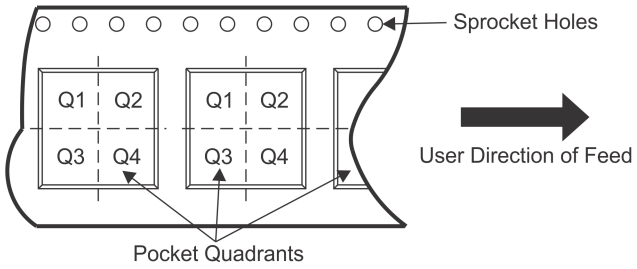


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

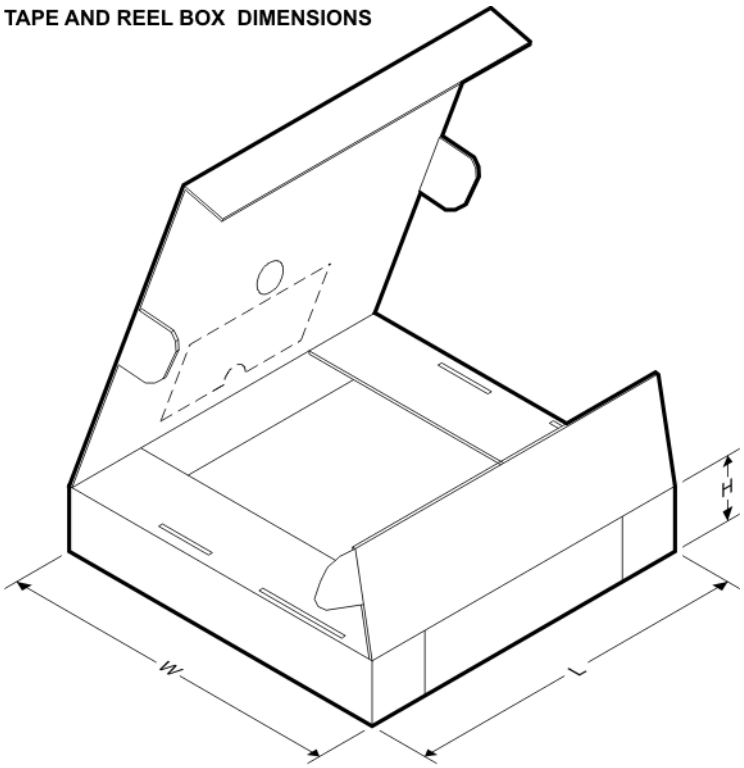
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51632RSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS51632RSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

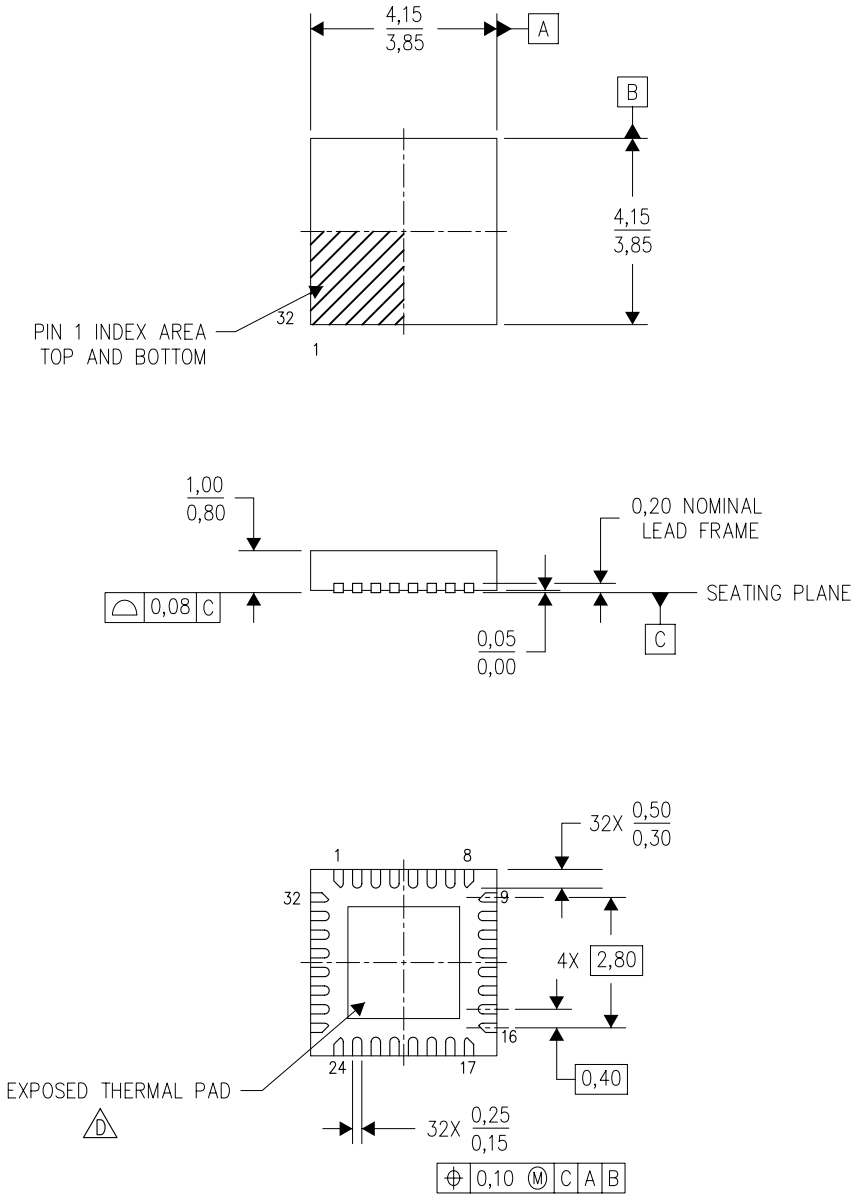
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51632RSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
TPS51632RSMT	VQFN	RSM	32	250	210.0	185.0	35.0

RSM (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



4207560/B 03/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

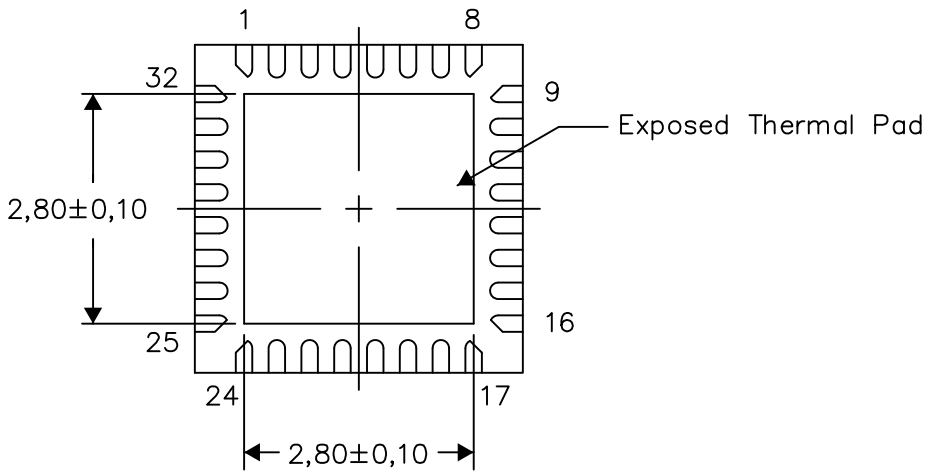
RSM (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



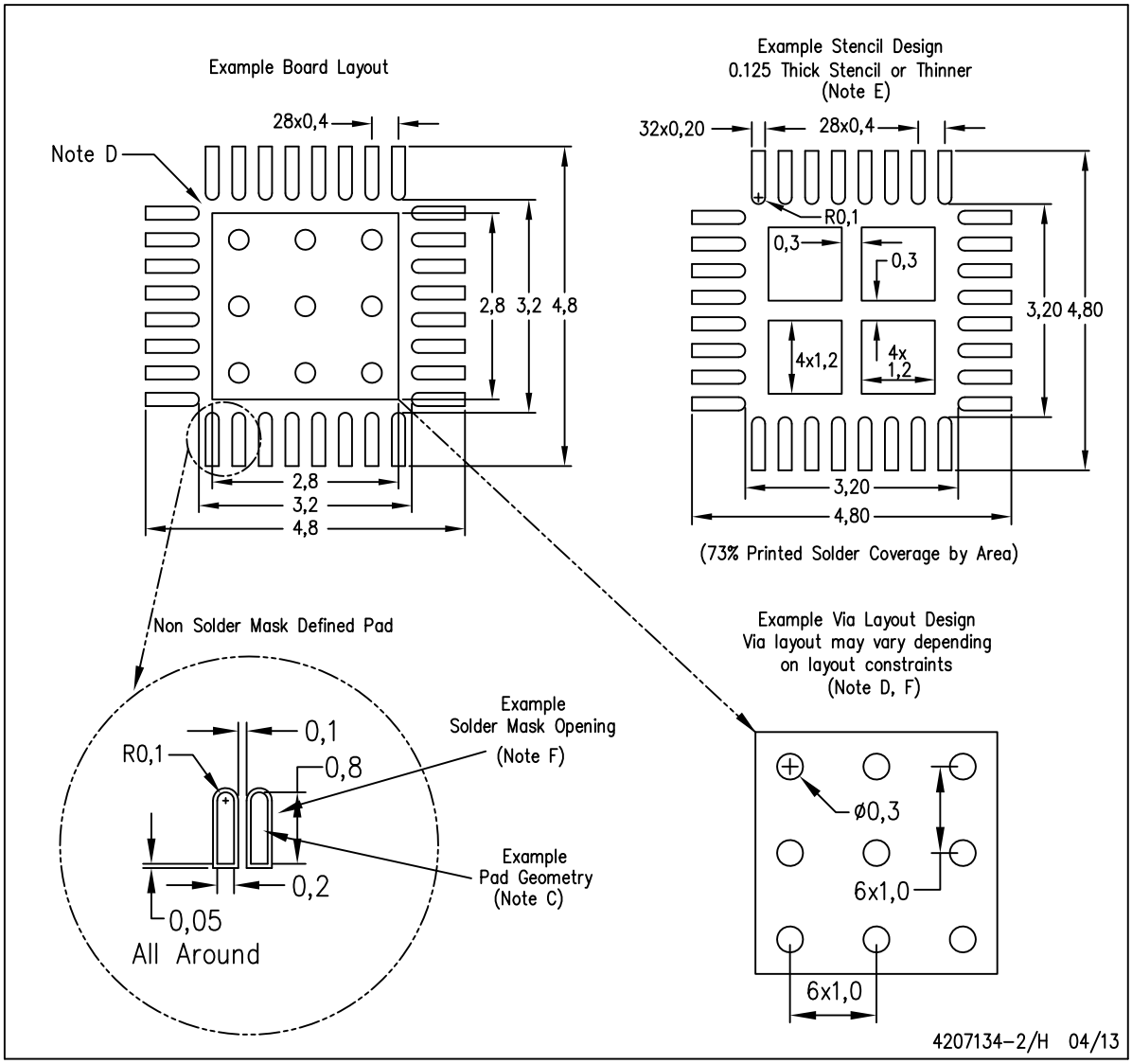
Bottom View

Exposed Thermal Pad Dimensions

4207868–2/H 04/13

NOTE: All linear dimensions are in millimeters

RSM (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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