

OPERAND INSTRUCTIONS INVOLVING IMMEDIATE DATA

MOV }
ADD/ADC/SUB/SBB } R/M, d8/d16
AND/OR/XOR/TEST/CMP

8 byte registers + 8 word registers + 24 byte
memory + 24 word memory = 64 opcodes

10 instructions x 64 = 640 opcodes

3.3.1 Move Immediate data to a Register/ Memory location

	Before	After		
MOV DX, ABCDH	DX <table border="1"><tr><td>1234H</td></tr></table>	1234H	<table border="1"><tr><td>ABCDH</td></tr></table>	ABCDH
1234H				
ABCDH				

	Before	After		
MOV BH, 12H	BH <table border="1"><tr><td>56H</td></tr></table>	56H	<table border="1"><tr><td>12H</td></tr></table>	12H
56H				
12H				

3.3.2 Add Immediate data to a Register/ Memory location

	Before	After		
ADD [BX], 12H	BX <table border="1"><tr><td>1000H</td></tr></table>	1000H		
1000H				
	DS:1000H <table border="1"><tr><td>20H</td></tr></table>	20H	<table border="1"><tr><td>32H</td></tr></table>	32H
20H				
32H				
	DS:1001H			

	Before	After		
ADD [BX], 1234H	BX <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>1000H</td></tr></table>	1000H		
1000H				
	DS:1000H <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>2000H</td></tr></table>	2000H	<table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>3234H</td></tr></table>	3234H
2000H				
3234H				
	DS:1002H			

3.3.3 Add with Carry Immediate data to a Register/ Memory location

	Before	After		
ADC DH, 32H	DH <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>30H</td></tr></table>	30H	<table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>63H</td></tr></table>	63H
30H				
63H				
Add with Carry	Carry flag <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>1</td></tr></table>	1	<table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>0</td></tr></table>	0
1				
0				

63H= 0110 0011 It has four 1's

New flag values: Ac=0, S=0, Z=0, V=0, P=1

3.3.4 Subtract Immediate data from a Register/ Memory location

	Before	After		
SUB DH, 40H	DH <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>30H</td></tr></table>	30H	<table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>F0H</td></tr></table>	F0H
30H				
F0H				

Subtract (without borrow)

F0H=1111 0000 B(Four 1's)

New flag values: Ac=0, S=1, Z=0, V=0, P=1, Cy=1

3.3.5 Subtract with borrow Immediate data from a Register/ Memory location

	Before	After
SBB DH, 25H	DH 20H	06H
Subtract (with borrow)	Cy flag 1	1

06H = 0000 0110B (Two 1's)

New flag values: Ac=1, S=0, Z=0, V=0, P=1, Cy=1

3.3.6 AND Immediate data with a Register/ Memory location

	Before	After
AND BH, 0FH	BH 56H	06H
56H = 0101 0110B	AND	
0FH = 0000 1111B	Cy flag 1	1
06H = 0000 0110B (Two 1's)		

Use: Selectively reset to 0 some bits of the destination

Bits that are ANDed with 0's are reset to 0

Bits that are ANDed with 1's are not changed

3.3.7 OR Immediate data with a Register/ Memory location

	Before	After
OR BH, 0FH	BH 56H	5FH
56H = 0101 0110B	OR	

0FH = 0000 1111B

CL

0FH

5FH = 0101 1111B

Use: Selectively set to 1 some bits of the destination

Bits that are ORed with 1's are set to 1

Bits that are ORed with 0's are not changed

3.3.8 Ex-OR Immediate data with a Register/ Memory location

		Before	After		
XOR BH, 0FH		BH <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>56H</td></tr></table>	56H	<table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>59H</td></tr></table>	59H
56H					
59H					
56H = 0101 0110B	XOR				
0FH = 0000 1111B		CL <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>0FH</td></tr></table>	0FH		
0FH					
59H = 0101 1001B					

Use: Selectively complement some bits of the destn.

Bits that are XORed with 1's are complemented

Bits that are XORed with 0's are not changed

3.3.9 Test immediate data with a Register/ Memory location

		Before	After		
TEST BH, 0FH		BH <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>56H</td></tr></table>	56H	<table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>56H</td></tr></table>	56H
56H					
56H					
56H=0101 0110B	AND				
0FH=0000 1111B		Temp <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>45H</td></tr></table>	45H	<table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>06H</td></tr></table>	06H
45H					
06H					

06H=0000 0110B

TEST basically performs AND operation. Result of AND is not stored in destination. It is stored in Temp register. Temp is not accessible to programmer. There is no instruction like MOV Temp, 67H. Only flags are affected.

Source : <http://elearningatria.files.wordpress.com/2013/10/cse-iv-microprocessors-10cs45-notes.pdf>