Chapter 5 : Processor Fundamentals

⟹ Central Processing Unit Architecture

→ Von Neumann model

→ Von Neumann architecture uses a single processor

→ it follows a linear sequence of FETCH - DECODE - EXECUTE

→ In order to do this, the processor uses registers

⟹ Registers

→ Smallest unit of storage of microprocessor ; allows fast data transfer between other registers.

→ General Purpose registers

→ Used to temporarily store data values which have been read from memory or some processed result

→ Can be used by assembly language instructions

→ Special Purpose registers

→ Some accessible by assembly language instructions

→ holds only data or memory location not both

ex. → Program Counter (PC) - holds address of next instruction to be fetched

→ Memory data register (MDR) - holds data value fetched from memory

→ Memory address register (MAR) - holds address of memory which is to be accessed

→ Accumulator (ACC) - holds all values that are processed by ALU

→ Index Register (IX) - stores a number used to change an address value

→ Current Instruction Register (CIR) - fetched program instruction is stored here for decoding and executing

→ Status Register - holds results of comparisons to decide later.

⟹ Processor CPU

→ Arithmatic and Logical unit (ALU) - processes everything related to arithmatic or logic

→ Control Unit (CU) - fetches instructions, decodes them and synchronizes operations

→ Immediate Access Store (IAS) - memory unit that can be directly accessed by processor

→ System Clock - timing device connected to processor that is needed to synchronize all components

⇒ Buses

- A set of wires that allow data transfer between components in a computer system.
- Data Bus
  - Bidirectional bus that carries data instructions between processor, memory and I/O devices
- Address Bus
  - Unidirectional bus that carries address of main memory location or input/output device about to be used
- Control Bus
  - Bidirectional and Unidirectional
  - used to transmit control signals from control unit

⇒ Factors affecting performance of computer system

- Clock Speed
  - Number of pulses the clock sends out in a given time interval / Number of processes CPU executes in a given time interval. Usually measured in Gigahertz (GH_z)
- Bus width
  - Number of bits that can be simultaneously transferred
- Cache memory
  - Commonly used instructions are stored in the cache memory
- Number of cores
  - Most CPU chips are multi-core. Each core processes different instruction simultaneously.

⇒ Ports

→ Hardware which provides a physical interface between a device with CPU and a peripheral device

→ Peripheral (I/O) devices cannot be directly connected to CPU hence connected through ports.

→ Universal serial Bus (USB) can connect both I/O devices to processor through USB port.

→ High definition Multimedia Interface (HDMI)

→ Can only connect output devices (ex. LCD)

→ HDMI cables transmit high-bandwidth and high-resolution video and audio streams

→ Video Graphics Array (VGA)

→ Can only connect output devices (ex. second monitor / display)

→ allows the transmission of video only no audio.

⇒ Fetch-Execute Cycle

→ Fetch Stage

→ PC holds address of next instruction to be fetched

→ Address in PC copied to MAR

→ PC is incremented

→ Instruction loaded to MDR from address held in MAR

→ Instruction from MDR loaded to CIR

→ Decode stage

→ The opcode and operand parts of instructions are identified

→ Execute Stage

→ Instructions executed by Control unit

⇒ Register Transfer Notation (RTN)

MAR ← [PC]

PC ← [PC] + 1

MDR ← [[MAR]]

CIR ← [MDR]

Decode

Execute

Return to start

Sq brackets: value currently in that register

double sq brackets: CPU must do a logical process and then copy this value.